This application note describes how to implement the Bus LVDS (BLVDS) interface in the supported Altera® device families for high-performance multipoint applications. This application note also shows the performance analysis of a multipoint application with the Cyclone® III BLVDS example.

The supported device families are:

- Arria® II
- Arria V
- Cyclone III (Cyclone III and LS devices)
- Cyclone IV
- Cyclone V
- Stratix® III
- Stratix IV
- Stratix V

The following topics are discussed in this application note:

- “BLVDS Overview”
- “BLVDS Technology in Altera Devices” on page 4
- “BLVDS Power Consumption” on page 7
- “Design Example” on page 8
- “Performance Analysis” on page 12

LVDS is becoming the most popular differential I/O standard for high-speed transmission in the industry.

The advantages of LVDS include high-noise tolerance in the form of common-mode rejection, low-power, and low-noise generation. Improved signal to noise rejection of LVDS allows the signal swing to operate at only a few hundred mV, which in turn allows faster data rates.

However, many high-speed applications require more than just point-to-point communication. The desire for multipoint communication has spawned a new variant of LVDS called BLVDS, which extends the capability of LVDS to multipoint configuration such as high-speed backplane applications. There are several bus topologies for the BLVDS I/O standard, such as multidrop bus with single or double termination, and multipoint.
**BLVDS Overview**

This section contains the calculations of the effective differential impedance of a fully loaded bus (referred to as effective impedance) and the propagation delay through the bus. Other multipoint BLVDS design considerations include fail-safe biasing, connector type and connector pinout, bus trace layout on the PCB, and driver edge rate specifications.

### BLVDS System

Figure 1 shows a typical multipoint BLVDS system which consists of a number of transmitter and receiver pairs (transceivers) that are connected to the bus.

![Figure 1. Multipoint BLVDS](image)

The configuration in Figure 1 provides bidirectional half-duplex communication while minimizing interconnect density.

Any transceiver can assume the role of a transmitter, with the remaining transceivers acting as receivers (only one transmitter can be active at a time). Bus traffic control, either through a protocol or hardware solution is typically required to avoid driver contention on the bus.

The performance of a multipoint BLVDS is greatly affected by the capacitive loading and termination on the bus.

### Effective Impedance

The effective impedance depends on the bus trace characteristic impedance $Z_o$ and capacitive loading on the bus. The connectors, the stub on the plug-in card, the packaging, and the receiver input capacitance all contribute to capacitive loading, which reduces the bus effective impedance.

Use Equation 1 to approximate the effective differential impedance of the loaded bus ($Z_{eff}$).

**Equation 1. Effective Differential Impedance**

\[
Z_{\text{eff}} = Z_{\text{eff}}^* \sqrt{\frac{C_o}{C_o + (NC_c / H)}}
\]

\[
= Z_{\text{eff}}^* \sqrt{\frac{C_o}{C_o + C_d}}
\]
Where:

- $Z_{\text{diff}} \ (\Omega) = 2 \times Z_0$ = the differential characteristic impedance of the bus
- $C_0 \ (\text{pF/inch})$ = characteristic capacitance per unit length of the bus
- $C_L \ (\text{pF})$ = capacitance of each load
- $N$ = number of loads on the bus
- $H$ (inch) = $d \times N$ = total length of the bus
- $d$ (inch) = spacing between each plug-in card
- $C_d \ (\text{pF/inch}) = C_L / d$ = distributed capacitance per unit length across the bus

The increment in load capacitance or closer spacing between the plug-in cards reduces the effective impedance. To optimize the system performance, it is important to select a low capacitance transceiver and connector. Keep each receiver stub length between the connector and transceiver I/O pin as short as possible.

Figure 2 shows the effects of distributed capacitance on normalized effective impedance.

Termination is required at each end of the bus, while the data flows in both directions. To reduce reflection and ringing on the bus, you must match the termination resistor to the effective impedance.

For a system with $C_d / C_0 = 3$, the effective impedance is 0.5 times of $Z_{\text{diff}}$. With double terminations on the bus, the driver sees an equivalent load of 0.25 times of $Z_{\text{diff}}$, and thus reduces the signals swing and differential noise margin across the receiver inputs (if standard LVDS driver is used). The BLVDS driver addresses this issue by increasing the drive current to achieve similar voltage swing at the receiver inputs.
**Propagation Delay**

The propagation delay \( t_{PD} = Z_o \times C_o \) is the time delay through the transmission line per unit length. It depends on the characteristic impedance and characteristic capacitance of the bus.

For a loaded bus, you can calculate the effective propagation delay with Equation 2. You can calculate the time for the signal to propagate from driver A to receiver B as the \( t_{PD\text{EFF}} \times \text{length of line between driver A and receiver B} \).

**Equation 2. Effective Propagation Delay**

\[
t_{PD\text{EFF}} = t_{PD} \times \sqrt{1 + \frac{C_s}{C_o}}
\]

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**BLVDS Technology in Altera Devices**

In supported devices, the **BLVDS** interface is supported in any row or column I/O banks that are powered by a \( V_{CCIO} \) of 2.5-V. The interface is supported on the differential I/O pins, but not the clock pins in these I/O banks.

The **BLVDS** transmitter uses two single-ended (SE) output buffers with the second output buffer programmed as inverted. The **BLVDS** receiver uses a dedicated **LVDS** input buffer.

In multidrop applications, either the input or output buffer is used, depending if the device is intended for driver or receiver operation. In multipoint applications, the output buffer and input buffer shares the same I/O pins. An output enable (\( oe \)) signal is required to tri-state the **LVDS** output buffer when it is not sending signals.

You should not enable the on-chip series termination (R, OCT) for the output buffer. Also, you should use external resistors at the output buffers to provide impedance matching to the stub on the plug-in card. You should not enable the on-chip differential termination (\( R_o \), OCT) for the differential input buffer because the bus termination is usually implemented using the external termination resistors at both ends of the bus.
Figure 3 shows the **BLVDS** I/O buffers in the supported devices.

**Figure 3. BLVDS I/O Buffers in the Supported Devices**

Cyclone III and Cyclone IV Devices

Table 1 lists the I/O standards and features for implementing **BLVDS** in Cyclone III and Cyclone IV devices.

**Table 1. I/O Standard and Features Support for the BLVDS Interface**

<table>
<thead>
<tr>
<th>Device</th>
<th>I/O Standard</th>
<th>Pin (1)</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt; (V)</th>
<th>Current Strength Option (mA)</th>
<th>Slew Rate</th>
<th>Overall Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone III</td>
<td>BLVDS</td>
<td>DIFFIO</td>
<td>2.5</td>
<td>8,12 (default), 16, 16</td>
<td>Slow</td>
<td>0</td>
</tr>
<tr>
<td>Cyclone IV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Medium</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Fast (default)</td>
<td>2</td>
</tr>
</tbody>
</table>

**Note to Table 1:**

(1) For more information about pin assignments, refer to the Cyclone III Pin-Out Files and Cyclone IV Pin-Out Files on the Altera website.

For more information about the **BLVDS** I/O features and electrical specifications, refer to the following documents:

- For Cyclone III devices:
  - *I/O Features in the Cyclone III Device Family* chapter of the Cyclone III Device Handbook
  - *Cyclone III Device Datasheet* chapter of the Cyclone III Device Handbook

- For Cyclone IV devices:
  - *I/O Features in Cyclone IV Devices* chapter of the Cyclone IV Device Handbook
  - *Cyclone IV Device Datasheet* chapter of the Cyclone IV Device Handbook
**Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V Devices**

Table 2 lists the I/O standards and features for implementing BLVDS in Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V devices.

### Table 2. I/O Standard and Features Support for the BLVDS Interface

<table>
<thead>
<tr>
<th>Device</th>
<th>I/O Standard (1)</th>
<th>Pin (2)</th>
<th>V&lt;sub&gt;CCIO&lt;/sub&gt; (V)</th>
<th>Current Strength Option (mA)</th>
<th>Slew Rate</th>
<th>Option Setting</th>
<th>Quartus II Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arria II, Stratix III, Stratix IV</td>
<td><strong>Differential SSTL-2 Class I</strong></td>
<td><strong>DIFFIO_RX</strong> (3)</td>
<td>2.5</td>
<td>8, 10, 12</td>
<td>8, 12</td>
<td>Slow</td>
<td>0</td>
</tr>
<tr>
<td>Arria V, Cyclone V, Stratix V</td>
<td><strong>Differential SSTL-2 Class I</strong></td>
<td><strong>DIFFIO_RX</strong> (3)</td>
<td>2.5</td>
<td>8, 10, 12</td>
<td>8, 12</td>
<td>Slow</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td><strong>Differential SSTL-2 Class II</strong></td>
<td><strong>DIFFIO_RX</strong> (3)</td>
<td>2.5</td>
<td>16</td>
<td>16</td>
<td>Fast (default)</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td><strong>Differential SSTL-2 Class II</strong></td>
<td><strong>DIFFIO_RX</strong> (3)</td>
<td>2.5</td>
<td>16</td>
<td>16</td>
<td>Fast (default)</td>
<td>3</td>
</tr>
</tbody>
</table>

**Notes to Table 2:**

1. You can implement the BLVDS interface with 2.5-V Differential SSTL Class I or II, depending on the current strength requirement.
2. For more information about pin assignments, refer to the Arria II GX Pin-Out Files, Arria V Pin-Out Files, Cyclone V Pin-Out Files, Stratix III Pin-Out Files, Stratix IV Pin-Out Files, and Stratix V Pin-Out Files on the Altera website.
3. DIFFIO_TX pins do not support true LVDS differential receivers.

For more information about the 2.5-V Differential SSTL I/O standard electrical specifications and features, refer to the following documents:

- For Arria II devices:
  - I/O Features in Arria II Devices chapter of the Arria II Device Handbook
  - Device Datasheet for Arria II Devices chapter of the Arria II Device Handbook

- For Arria V devices:
  - I/O Features in Arria V Devices chapter of the Arria V Device Handbook
  - Arria V Device Datasheet

- For Cyclone V devices:
  - I/O Features in Cyclone V Devices chapter of the Cyclone V Device Handbook
  - Cyclone V Device Datasheet
For Stratix III devices:

- **Stratix III Device I/O Features** chapter of the *Stratix III Device Handbook*
- **DC and Switching Characteristics for Stratix III Devices** chapter of the *Stratix III Device Handbook*

For Stratix IV devices:

- **I/O Features in Stratix IV Device** chapter of the *Stratix IV Device Handbook*
- **DC and Switching Characteristics for Stratix IV Devices** chapter of the *Stratix IV Device Handbook*

For Stratix V devices:

- **I/O Features in Stratix V Devices** chapter of the *Stratix V Device Handbook*
- **Stratix V Device Datasheet**

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**BLVDS Power Consumption**

When compared with other high-performance bus technologies, such as GTL that uses more than 40 mA, BLVDS typically drives out current in the range of 10 mA.

For example, based on the Cyclone III PowerPlay Early Power Estimator (EPE) estimation for typical power characteristics of Cyclone III devices in an ambient temperature of 25°C, the average power consumption of a BLVDS bidirectional buffer at a data rate of 50 MHz and an output enabled 50% of the time is approximately 17 mW.

Before implementing your design into the device, use the Excel-based EPE for the supported device you use to get an estimated magnitude of the BLVDS I/O power consumption.

For input and bidirectional pins, the BLVDS input buffer is always enabled. The BLVDS input buffer consumes power if there is switching activity on the bus (for example, other transceivers are sending and receiving data, but the Cyclone III device is not the intended recipient).

If you use BLVDS as an input buffer in multidrop or as a bidirectional buffer in multipoint applications, Altera recommends entering a toggle rate that includes all activities on the bus, not just activities intended for the Altera device BLVDS input buffer.

**Example 1** shows the BLVDS I/O entry in the Cyclone III EPE. For Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V devices, select **2.5-V Differential SSTL Class I** or **Class II** under the I/O standard column in the Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V EPE.

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**Example 1. Example of BLVDS I/O Data Entry in the Cyclone III EPE 9.0 SP2**

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>Current Strength / Output Termination</th>
<th>Slower Rate</th>
<th>Input Pins</th>
<th>Output Pins</th>
<th># Bidir Pins</th>
<th>Data Rate</th>
<th>Clock freq (MHz)</th>
<th>Toggle %</th>
<th>OF</th>
<th>Eg</th>
<th>Lead (pF)</th>
<th>Routing</th>
<th>Block</th>
<th>Total</th>
<th>ICEXT</th>
<th>ICDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus LVDS</td>
<td>12mA</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>DDR</td>
<td>100.0</td>
<td>50.0%</td>
<td>0.0%</td>
<td>5</td>
<td>0.001</td>
<td>0.165</td>
<td>0.165</td>
<td>0.012</td>
<td>0.103</td>
<td></td>
</tr>
<tr>
<td>2.5 V</td>
<td>4mA</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>DDR</td>
<td>400.0</td>
<td>50.0%</td>
<td>100%</td>
<td>5</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
</tr>
</tbody>
</table>
Altera recommends using the Quartus® II PowerPlay Power Analyzer to perform an accurate BLVDS I/O power analysis after you complete your design. The PowerPlay Power Analyzer estimates power based on the specifics of the design after place-and-route is completed. The PowerPlay Power Analyzer applies a combination of user-entered, simulation-derived, and estimated signal activities which, combined with the detailed circuit models, yields very accurate power estimates.

For more information about the EPE and the Quartus II PowerPlay Power Analyzer, refer to the following documents:

- PowerPlay Power Analysis chapter of the Quartus II Handbook.
- PowerPlay Early Power Estimator (EPE) and Power Analyzer page on the Altera website.

**Design Example**

The design example shows you how to instantiate the BLVDS I/O buffer in the supported devices with the ALTIOBUF megafnction in the Quartus II software.

When instantiating the BLVDS I/O buffer, Altera recommends you to specify the following in your design:

- Two SE output buffers with the oe signal controlled by the same signal (refer to step 1)
- A differential input buffer (refer to step 2)
- A signal splitter that connects two SE output buffers (refer to step 3)
- Assign one of the following I/O standards to the bidirectional pins (refer to step 4 and 5):
  - BLVDS I/O standard for Cyclone III or Cyclone IV devices
  - 2.5-V Differential SSTL Class I or Class II for Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, or Stratix V devices

During a write operation, the BLVDS I/O buffer functions as follows:

- Receive a serial data stream from the FPGA core through the dout\_p input port
- Create an inverted version of the data
- Transmit the data through the two SE output buffers connected to the \( p \) and \( n \) bidirectional pins

During a read operation, the differential input buffer functions as follows:

- Receives the data from the bus through the \( p \) and \( n \) bidirectional pins
- Sends the serial data to the FPGA core through the din port

The oe port receives the oe signal from the FPGA core to enable or disable the SE output buffers. Keep the oe signal low to tri-state the output buffers during read operation. The function of the AND gate is to stop the transmitted signal from going back into the FPGA core. The differential input buffer is always enabled.
Figure 4 shows the block diagram of the design example in the Quartus II software.

**Figure 4. Block Diagram of the Design Example in the Quartus II Software**

For more information about the ALTIOBUF megafunction, refer to the *I/O Buffer Megafunction (ALTIOBUF) User Guide*.

You can download the design examples from the *Design Examples for AN 522* on the Altera website.

For more information about creating a new project in the Quartus II software using the MegaWizard™ Plug-In Manager, refer to the *Megafunction Overview User Guide*. 
Design Example Guidelines

The following steps describe the design flow for the design example that uses a Cyclone III device. They are applicable to all the supported devices. Make sure you select the right device.

1. To create the SE output buffers, instantiate the ALTIOBUF megafuntion with the MegaWizard Plug-In Manager. Configure the module As an output buffer, enter 1 for the What is the number of buffers to be instantiated box, and turn on Use output enable port(s).

2. To create the differential input buffer, instantiate the ALTIOBUF megafunction. Configure the module As an input buffer, enter 1 for the What is the number of buffers to be instantiated box, and turn on Use differential model.

3. Instantiate the signal splitter function. In the Edit menu, select Insert Symbol. Under the Project directory, select pdo symbol.

This is a custom function that comes with the design example. By using this function, the inversion of the data input from the core is implemented in the I/O element (IOE) to ensure minimum skew between the p and n output signals.

In the pdo.v file, modify the module instantiation of <family_name>_pseudo_diff_out with the respective device family name as follows:

- Arria II: arriaii
- Arria V: arriav
- Cyclone III: cycloneiii
- Cyclone III LS: cycloneiiils
- Cyclone V: cyclonev
- Stratix III: stratixiii
- Stratix IV: stratixiv
- Stratix V: stratixv

4. Connect the modules and the input and output ports, as shown in Figure 4.

5. In the Assignment Editor, assign the BLVDS I/O standard to the bidirectional p and n pins for Cyclone III and Cyclone IV devices, as shown in Figure 5. For Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, and Stratix V devices, assign 2.5-V Differential SSTL Class I or II. You can also set the current strength and slew rate options. Otherwise, the Quartus II software assumes the default settings.
Figure 5 shows the Quartus II Assignment Editor for BLVDS I/O assignment.

### Figure 5. BLVDS I/O Assignment in the Quartus II Assignment Editor

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
<th>Assignment Name</th>
<th>Value</th>
<th>Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>I/O Standard</td>
<td>Bus LVDS</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>n</td>
<td>I/O Standard</td>
<td>Bus LVDS</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>p</td>
<td>Slow Rate</td>
<td>2</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>n</td>
<td>Slow Rate</td>
<td>2</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>p</td>
<td>Current Strength</td>
<td>SMA</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>n</td>
<td>Current Strength</td>
<td>SMA</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>p</td>
<td>Location</td>
<td>FIL_T19</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>n</td>
<td>Location</td>
<td>FIL_T20</td>
<td></td>
<td>Yes</td>
</tr>
</tbody>
</table>

You can manually assign both the p and n pin locations for each supported device with the Assignment Editor (refer to Figure 5). The supported devices and the pins you can manually assign are as follows:

- Cyclone III, Cyclone IV: DIFFIO
- Arria II, Arria V, Cyclone V, Stratix III, Stratix IV, Stratix V: DIFFIO_RX

6. Compile and perform functional simulation with the ModelSim-Altera software. Figure 6 illustrates the simulation waveforms.

### Figure 6. Example of Functional Simulation Results

Note to Figure 6:
(1) When the oe signal is asserted, the BLVDS is in the write operation mode. When the oe signal is de-asserted, the BLVDS is in the read operation mode.

For more information about the ModelSim-Altera software, refer to the ModelSim-Altera Software Support section on the Altera website. The section contains various links to topics such as installation, usage, and troubleshooting.

For simulation using Verilog HDL, you can use the “blvds_tb.v” testbench, which is included in the respective design example.
Performance Analysis

This section contains the performance analysis of a multipoint BLVDS based on the Cyclone III BLVDS input output buffer information specification (IBIS) model simulation in HyperLynx. The performance analysis demonstrates the impact of the bus termination, loading, driver and receiver characteristics, and the location of the receiver from the driver on the system.

Altera recommends using a Stratix III, Stratix IV, or Stratix V 2.5-V Differential SSTL IBIS model for the simulation if you use Stratix III, Stratix IV, or Stratix V devices.

You can download Altera device models at the Altera IBIS Model page on the Altera website.

System Setup

Figure 7 shows the schematic of a multipoint topology with 10 Cyclone III BLVDS transceivers (named U1 to U10).

The bus transmission line is assumed to have the following characteristics:

- A stripline
- Characteristic impedance of 50 Ω
- Characteristic capacitance of 3.6 pF per inch
- Length of 10 inches
- Bus differential characteristic impedance of approximately 100 Ω
- Spacing between each transceiver of 1 inch
- Bus terminated at both ends with termination resistor RT

Figure 7. Multipoint BLVDS with Cyclone III BLVDS Transceivers
In the example shown in Figure 7, the fail-safe biasing resistors of 130 kΩ and 100 kΩ pulls the bus to a known state when all the drivers are tri-stated, removed, or powered off.

To prevent excessive loading to the driver and waveform distortion, the magnitude of the fail-safe resistors must be one or two orders higher than $R_T$. To prevent a large common-mode shift from occurring between the active and tri-state bus conditions, the mid-point of the fail-safe bias must be close to the offset voltage of the driver (+1.25 V). You can power up the bus with the common power supplies ($V_{CC}$).

Cyclone III and Cyclone IV BLVDS transceivers are assumed to have the following characteristics:

- Default drive strength of 12 mA
- Slow slew rate settings by default
- Pin capacitance of each transceiver of 6 pF
- Stub on each BLVDS transceiver is a 1-inch microstrip of characteristic impedance of 50 Ω and characteristic capacitance of 3 pF per inch
- Capacitance of the connection (connector, pad, and via in PCB) of each transceiver to the bus is assumed to be 2 pF
- Total capacitance of each load is approximately 11 pF

For 1-inch load spacing, the distributed capacitance is equal to 11 pF per inch. To reduce reflection caused by the stubs, and also to attenuate the signals coming out of the driver, an impedance matching 50 Ω resistor $R_s$ is placed at the output of each transceiver.
**Bus Termination**

The effective impedance of the fully loaded bus is 52 Ω if you substitute the bus characteristic capacitance and the distributed capacitance per unit length of the setup into Equation 1 on page 2. For optimum signal integrity, you must match $R_t$ to 52 Ω.

Figure 8 through Figure 11 show the effects of matched-, under-, and over-termination on the differential waveform ($V_{ID}$) at the receiver input pins. The data rate is 100 Mbps.

For Figure 8 and Figure 9, U1 acts as the transmitter and U2 to U10 are the receivers, whereas for Figure 10 and Figure 11, U5 is the transmitter and the rest are receivers. For both cases, under-termination ($R_t = 25$ Ω) results in reflections and significantly reduction of the noise margin. In some cases, under termination even violates the receiver threshold ($V_{TH} = \pm 100$ mV). When $R_t$ is changed to 50 Ω there is a substantial noise margin with respect to $V_{TH}$ and the reflection is negligible.

**Figure 8. Effect of Bus Termination (Driver in U1, Receiver in U2)**

![Figure 8. Effect of Bus Termination (Driver in U1, Receiver in U2)](image)
Figure 9. Effect of Bus Termination (Driver in U1, Receiver in U10)
Figure 10. Effect of Bus Termination (Driver in U5, Receiver in U6)
The relative position of the driver and receiver on the bus also affects the received signal quality. The nearest receiver to the driver experiences the worst transmission line effect because at this location, the edge rate is the fastest. This is made worse when the driver is located at the middle of the bus.

For example, compare Figure 8 and Figure 10. \( V_{id} \) at receiver U6 (driver at U5) shows larger ringing than that at receiver U2 (driver at U1). On the other hand, the edge rate is slowed down when the receiver is located further away from the driver. The largest rise time recorded is 1.14 ns with the driver located at one end of the bus (U1) and the receiver at the other end (U10).
### Stub Length

Figure 12 compares the $V_{id}$ at U10 when the stub length is increased from one inch to two inches and the driver is at U1.

Longer stub length not only increases the flight time from the driver to the receiver, but also results in a larger load capacitance, which causes larger reflection.

Figure 12. Effect of Increasing Stub Length (Driver in U1, Receiver in U10)
**Stub Termination**

You must match the driver impedance to the stub characteristic impedance. Placing a series termination resistor $R_s$ at the driver output greatly reduces the adverse transmission line effect caused by long stub and fast edge rates. In addition, $R_s$ can be changed to attenuate the $V_{ID}$ to meet the specification of the receiver.

Figure 13 compares the $V_{ID}$ at U2 and U10 when U1 is transmitting.

**Figure 13. Effect of Stub Termination (Driver in U1, Receiver in U2 and U10)**
Driver Slew Rate

Figure 14 shows the driver slew rate effect. A comparison is made between the slow and fast slew rate with a 12 mA drive strength. The driver is at U1 and the differential waveforms at U2 and U10 are examined.

A fast slew rate helps to improve the rise time, especially at the receiver furthest from the driver. However, a faster slew rate also magnifies ringing due to reflection.

Figure 14. Effect of Driver Edge Rate (Driver in U1, Receiver in U2 and U10)
Overall System Performance

The highest data rate supported by a multipoint BLVDS is determined by looking at the eye diagram of the furthest receiver from a driver. At this location, the transmitted signal has the slowest edge rate and affects the eye opening. Although the quality of the received signal and the noise margin goal depend on the applications, the wider the eye opening, the better. However, you must also check the receiver nearest to the driver, because the transmission line effects tend to be worse if the receiver is located closer to the driver.

Figure 15 illustrates the eye diagrams at U2 (red curve) and U10 (blue curve) for a data rate at 400 Mbps. Random jitter of a 1% unit interval is assumed in the simulation. The driver is at U1 with default current strength and slew rate settings. The bus is fully loaded with optimum $R_t = 50 \, \Omega$. The smallest eye opening is at U10, which is furthest from U1. The eye height sampled at the 0.5 unit interval is 692 mV and 543 mV for U2 and U10, respectively. There is a substantial noise margin with respect to $V_{TH} = \pm 100$ mV for both cases.

Figure 15. Eye Diagram at 400 Mbps (Driver in U1, Receiver in U2 and U10)
Summary

The multipoint BLVDS offers an efficient solution for multipoint backplane applications. A good multipoint design must consider the capacitive load and termination on the bus to obtain better signal integrity. You can minimize the load capacitance by selecting a transceiver with low pin capacitance, connector with low capacitance, and keeping the stub length short.

Arria II, Arria V, Cyclone III, Cyclone IV, Cyclone V, Stratix III, Stratix IV, and Stratix V devices provide a solution to the implementation of the BLVDS interface in multipoint backplane applications.

In addition, the programmable features of the drive strength and slew rate options enable system designers to customize their multipoint system for maximum performance. To determine the maximum data rate supported, you must perform a simulation or measurement based on your specific system setup and application.

Document Revision History

Table 3 lists the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tr>
<td>June 2012</td>
<td>2.2</td>
<td>■ Updated to include Arria II, Arria V, Cyclone V, and Stratix V devices.</td>
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<td></td>
<td></td>
<td>■ Updated Table 1 and Table 2.</td>
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<tr>
<td>April 2010</td>
<td>2.1</td>
<td>Updated the design example link in the “Design Example” section.</td>
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<tr>
<td>November 2009</td>
<td>2.0</td>
<td>■ Included Arria II GX, Cyclone III, and Cyclone IV device families in this application note.</td>
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<tr>
<td></td>
<td></td>
<td>■ Updated Table 1, Table 2, and Table 3.</td>
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<td></td>
<td>■ Update Figure 5, Figure 6, Figure 8 through Figure 11.</td>
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<tr>
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<td>■ Updated design example files.</td>
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<tr>
<td>November 2008</td>
<td>1.1</td>
<td>■ Updated to new template</td>
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<td></td>
<td></td>
<td>■ Updated “BLVDS Technology in Altera Devices” chapter</td>
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<td>■ Updated “Power Consumption of BLVDS” chapter</td>
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<td>■ Updated “Design Example” chapter</td>
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<td></td>
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<td>■ Replaced Figure 4 on page 7</td>
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<td></td>
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<td>■ Updated “Design Example Guidelines” chapter</td>
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<td>■ Updated “Bus Termination” chapter</td>
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<td>■ Updated “Summary” chapter</td>
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<tr>
<td>July 2008</td>
<td>1.0</td>
<td>Initial release.</td>
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