Application Note
for Switching Mode Power Supply Design with 900V Switching Regulator—MP110

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ABSTRACT

This paper presents design guidelines for switching mode power supply using 900V switching regulator-MP110 from MPS, including Flyback and Buck converter as shown in Figure-1 and Figure-2. MP110 is the industry's first 900V monolithic regulator. A programmable PWM controller and 900V planar power MOSFET are combined in single chip. The design is quite simple and straightforward with the help of step-by-step design procedure described in this application note. Experimental results based on the design example are also presented in the last part of section 3 and section 4.

Figure-1 Flyback Converter with 900V Switching Regulator—MP110

Figure-2 Buck Converter with 900V Switching Regulator—MP110
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1. MP110 INTRODUCTION

MP110 is a monolithic regulator with programmable pulse width modulation (PWM) controller, 900V power MOSFET and high voltage current source in one chip. Based on the PWM technique, the switching frequency is fixed and doesn’t have much influence on other frequency band. When the load is below a given level, the regulator enters burst mode. As a result, it is prone to be used in the applications that are sensitive to noise, or need excellent light load efficiency and no load power consumption. Internal Vcc Under Voltage Lockout (UVLO), Over Load Protection (OLP), Vcc Over Voltage Protection (Vcc OVP), Short Circuit Protection (SCP), Input Over Voltage Protection (Input OVP) and Thermal Shutdown (TSD) are all implemented in the IC to provide full protection features and minimize the external component count. This paper presents practical design guidelines for off-line Flyback converter and Buck converter employing MP110. Step-by-step design procedure for PWM controlled Flyback converter and Buck converter using MP110 is introduced in this application note, mainly including transformer design, output filter design, component selection, thermal consideration, PCB layout and EMI design.

2. PULSE WIDTH MODULATION (PWM) CONTROL INTRODUCTION

PWM control is typical fixed frequency control scheme for Flyback converter. By implementing a fixed switching frequency mode control, the switching frequency is fixed and the peak current is regulated by FB voltage according to the required output power. During the ON time of the MOSFET, the Drain-Source current increases. Once the current reaches the regulated peak current limit, the MOSFET is turned off. The peak current limit decreases as the output power decreases. If the output power decreases in further, the controller enters burst mode for lower no load power consumption.

The switching frequency of MP110 is programmable and can be set up to 300kHz. It is easy to set the proper switching frequency to avoid specified frequency band.

Figure-3 shows the Drain-Source voltage waveform of primary switch in a PWM control Flyback converter. During the ON time of MOSFET, the Drain-Source current increases linearly until the peak current limit is reached. Then the MOSFET turns off. The leakage inductance of the Flyback transformer rings with the parasitic capacitance and causes a high voltage spike, which should be limited by a clamping circuit. When the one cycle elapses, the MOSFET turns on again and next period begins.
3. FLYBACK CONVERTER DESIGN PROCEDURE

A. Predetermined Input and Output Specifications

- Input AC voltage range: $V_{ac(min)}$, $V_{ac(max)}$, for example $85V_{ac}\sim420V_{ac}$ RMS
- DC bus voltage range: $V_{in(min)}$, $V_{in(max)}$.
- Output: $V_o$, $I_o(min)$, $I_o(max)$, $P_{out}$
- Estimated efficiency: $\eta$, It is used to estimate the power conversion efficiency to calculate the maximum input power. If there is no reference data, $\eta$ is set to be 0.7~0.75 for low output voltage applications and 0.8~0.85 for high output voltage applications.
- Estimated efficiency of transformer to output: $\eta_{ps}$, 0.85 for low output voltage applications and 0.9 for high output voltage applications.

Then the maximum input power can be given as:

$$P_{in} = \frac{P_{out}}{\eta} \quad (1)$$
Figure-4 shows the typical DC bus voltage waveform. The DC input capacitor $C_{in}$ is usually set as $2\mu F/W$ for the universal input condition. For 230V single range application, the capacitance can be half the value.

From the waveform above, the DC input Voltage $V_{DC}$ can be got as:

$$V_{DC}(V_{ac}, t) = \sqrt{2 \cdot V_{ac}^2 - \frac{2 \cdot P_{in}}{C_m} \cdot t}$$  \hspace{1cm} (2)

By setting $V_{AC} = V_{DC}$, $T1$ where DC bus voltage reaches to its minimum value $V_{DC(min)}$ can be calculated as

$$V_{DC(min)} = V_{DC}(V_{ac(min)}, T1)$$ \hspace{1cm} (3)

Then, the minimum average DC input voltage $V_{in(min)}$ can be derived as:

$$V_{in(min)} = \frac{\sqrt{2} \cdot V_{ac(min)} + V_{DC(min)}}{2}$$ \hspace{1cm} (4)

The maximum DC input voltage $V_{in(max)}$ can be got as:

$$V_{in(max)} = \sqrt{2} \cdot V_{ac(max)}$$ \hspace{1cm} (5)

According to the calculation above, the maximum voltage is $594V_{DC}$ and the maximum voltage rating of electrolytic capacitor is usually $400V$ or $450V$, so two electrolytic capacitors are needed for application with such high input voltage. The two electrolytic capacitors should stack as input filter. The capacitance of two stacked capacitors is equal to half value of each one. So the capacitance of each stacked capacitor should be double of the calculated capacitance. Also balancing resistors are needed in parallel with the capacitors. The structure of input capacitors is shown in Figure-5.
Both C1 and C2 endure half of input DC voltage. The R1~R4 should be used with the same resistance to balance the C1, C2 voltage stress. And the R1~R4 is recommended to use the 1206 package considering safety requirement. Also, the R1~R4 value should be large enough for energy saving. For example, 20MΩ balancing resistor consumes about 18mW at 600VDC bus voltage.

B. Determine the Startup Circuitry

Figure-6 shows the startup circuit. When power is supplied, the internal high voltage current source (typical 2mA) charges C1 through Drain of MP110. Once VCC voltage reaches 11.7V, the internal high voltage current source (2mA) turns off and IC starts switching, then the auxiliary winding takes over the power supply. If VCC drops below 8.0V before the auxiliary winding takes over the power supply, the switching stops and the internal high voltage current source turns on again, which re-charges the VCC.
external capacitor C1, another start-up procedure starts (see Figure-7).

Figure-7 Startup Waveform and VCC UVLO of MP110

C. Turns Ratio-N, Primary MOSFET and Secondary Rectifier Diode Selection

Figure-8 shows the typical voltage waveform of the MP110 Drain-Source and secondary rectifier diode in a Flyback converter. From the waveform, the primary Drain-Source voltage rating $V_{ds}$ can be derived as,

$$V_{ds} = V_{in(max)} + N \cdot (V_D + V_F) + 60V$$  \hfill (6)

Where $V_F$ is the forward voltage of the rectifier diode, 60V spike voltage is assumed here. The secondary rectifier diode voltage rating $V_{ka}$ can be estimated as equation (7):

$$V_{ka} = \frac{V_{in(max)}}{N} + V_D$$  \hfill (7)
From equation (6) and (7), the voltage rating for MP110 Drain-Source and secondary rectifier diode versus turns-ratio N can be calculated and their relationship is shown in Figure-9.

Generally, 10% voltage margin needs to be left for primary MOSFET and secondary rectifier diode. For example, in 90Vac~420Vac input, 12V output adapter application, the turn ratio N can be selected from 8-12 and 100V rectifier diode is preferred for better performance. N=9 or 10 is preferred to be selected considering MP110 and secondary rectifier diode voltage derating.
D. Determine Switching Frequency

The switching frequency of MP110 is programmable and maximum switching frequency is 300kHz. Higher switching frequency means smaller transformer core and tighter PCB area, but brings larger switching loss.

![Figure-10 Turn-On and Turn-Off Loss](image)

Figure-10 shows the turn-on and turn-off loss during switching period. The large current spike during turn on is caused by the large parasitic capacitance of 900V integrated MOSFET and the transformer. So the turn-on loss is much larger than turn-off loss at high line for MP110. Suppose the turn-on loss in T0-T1 is $E_{ON}$ and the turn-off loss in T2-T3 is $E_{OFF}$, the total switching loss can be calculated as equation (8).

$$P_s = (E_{ON} + E_{OFF}) \cdot f_s$$  \hspace{1cm} (8)

Where $f_s$ is the switching frequency.

Conducted EMI should be other aspect to be considered. The conducted EMI swept frequency range is from 150kHz-30MHz, and doesn't let 2nd harmonic fall in this range is a good choice. Generally, around 65kHz switching frequency is recommended for MP110 when the output power is about 5W or higher. Higher switching frequency can be set to achieve higher power density and tight dimension, if the output power is low. The switching frequency can be set simply by choosing the FSET resistor. The relationship of FSET resistor and switching frequency is shown as equation (9).

$$f_s = \frac{1}{200 \times 10^{-9} + 112.5 \times 10^{-12} \times \frac{R_{FSET}}{V_{FSET}}} \text{Hz}$$  \hspace{1cm} (9)

Where $V_{FSET}$ (typical 1.23V) is the reference voltage of FSET.

MP110 also provides the frequency jittering function which can simplifies the EMI input filter design. MP110 has the optimized frequency jittering with ±4% frequency deviation and 256Ts carrier cycle, which can effectively improve EMI performance.
E. Current Sensing Resistor Design

The peak current is sensed by a sensing resistor. The peak current limit increases as the load increases, and is controlled by FB voltage, as shown in Figure-11.

![Figure-11 Relationship of Current Sensing Voltage and Load](image)

The relation between peak current limit and FB voltage is,

\[
V_{\text{peak sense}} \div V_{\text{IR}} = I_{\text{div}}
\]

Where \( I_{\text{div}} \) is the FB current-set-point division ratio.

The maximum peak current limit is internally set to be 0.96V, and in order to avoid the sub-harmonic oscillation in Continuous Conduction Mode (CCM), the slope compensation function is implemented in the chip. The primary side peak current can be set by choosing proper current sensing resistor.

![Figure-12 Slope Compensation Waveform](image)

Figure-12 shows the relationship of peak current sensing voltage and the primary side ON time when MP110 delivers the maximum power. When the sum of the sensing voltage and the slope compensation voltage reaches the internal peak current limit \( V_{\text{CS}} \) (0.96V, typical), MP110 turns off the internal MOSFET. The maximum peak current limit is \( V_{\text{CS}} \) and the slope compensation slew rate \( S_{\text{Ramp}} \) is 40mV/\( \mu \)s. Considering the margin, use 95% of maximum peak current sensing level as the peak current limit at full load. The voltage on sensing resistor can be derived as,

\[
V_{\text{sense}} = 0.95 \cdot 0.96V - S_{\text{Ramp}} \cdot T_{\text{ON}}
\]

Where \( T_{\text{ON}} \) should be the MP110 maximum ON time at low line.

With a given power supply spec, the converter operation mode need to be selected firstly. Usually, BCM (Boundary Current Mode) is preferred for the low output power application. CCM is selected when the power level is high. The higher the power delivers, the deeper CCM should be adopted for higher...
efficiency and better thermal performance. But it must be kept in mind that the deeper CCM means larger transformer core.

If power supply is designed to operate in BCM at low line, it operates in DCM at high line. The magnetizing inductor current (the primary inductor current when primary side is turned on, and the current reflected to the primary side when secondary side diode on) and the Drain-Source voltage of MP110 is shown as Figure-13.
Since the primary side switching ON time decreases as the input voltage increases, the parameters should be designed at low line to guarantee the converter can deliver the required output power.

Since N has been selected, so if the power supply is designed to operate in boundary current mode (BCM) at low line, the peak current can be calculated easily as equation (12).

$$I_{\text{peak\_BCM}} = \frac{2 \cdot I_o}{N \cdot (1 - D_{\text{Vin\_min}})} \quad (12)$$

Where D is the duty of the switching, it can be derived from equation (13).

$$D_{\text{Vin\_min}} = \frac{(V_o + V_F) \cdot N}{V_{\text{in\_min}} + (V_o + V_F) \cdot N} \quad (13)$$

Where $V_F$ is the forward voltage drop of secondary side diode.

The ON time at low line can be calculated according to equation (14).

$$T_{\text{ON}} = \frac{D_{\text{Vin\_min}}}{f_s} \quad (14)$$

Then the sensing voltage $V_{\text{Sense}}$ and peak current $I_{\text{peak\_BCM}}$ can be calculated based on equation (11), (13) and (14), and sensing resistor can be got by equation (15).

$$R_{\text{Sense}} = \frac{V_{\text{Sense}}}{I_{\text{peak\_BCM}}} \quad (15)$$

If the peak current set by current sensing resistor is larger than $I_{\text{peak\_BCM}}$, the power supply always works in DCM. Otherwise, the power supply may enter CCM as Figure-14 shows. Here, $K_{\text{depth}}$ is defined as the depth of CCM.

$$K_{\text{depth}} = \frac{\Delta I}{I_{\text{peak}}} \quad (16)$$

![Figure-14 Primary Side Current in CCM](image-url)
So peak current can be got as equation (17).

\[ I_{\text{peak, CCM}} = \frac{2 \cdot l_b}{(1 - D) \cdot (1 + K_{\text{depth}}) \cdot N} \]  

(17)

If the CCM operation is adopted, please choose proper \( K_{\text{depth}} \) firstly. \( I_{\text{peak}} \) and \( I_{\text{valley}} \) can be calculated then. And the current sensing resistor could be selected by equation (18).

\[ R_{\text{sense}} = \frac{V_{\text{sense}}}{I_{\text{peak, CCM}}} \]  

(18)

Where \( V_{\text{sense}} \) is same as in equation (15).

The current sensing resistor with the proper power rating should be chosen based on the power loss given in equation (19) and equation (20) when converter operates in DCM and CCM.

\[ P_{\text{sense, BCM}} = I_{\text{peak}} \cdot \frac{D}{3} \cdot R_{\text{sense}} \]  

(19)

\[ P_{\text{sense, CCM}} = \left[ \left( \frac{I_{\text{peak}} + I_{\text{valley}}}{2} \right)^2 + \frac{1}{12} \left( I_{\text{peak}} - I_{\text{valley}} \right)^2 \right] \cdot D \cdot R_{\text{sense}} \]  

(20)

F. Primary Side Inductance \( L_m \) Design

The maximum power that a Flyback converter can deliver is related to the energy stored in the primary side inductance \( L_m \) as given in equation (21) and (22) for CCM and DCM respectively.

\[ \frac{1}{2} \cdot L_m \cdot (I_{\text{peak}}^2 - I_{\text{valley}}^2) \cdot f_s = \frac{P_{o, \text{CCM}}}{\eta_{\text{ps}}} \]  

(21)

\[ \frac{1}{2} \cdot L_m \cdot I_{\text{peak}}^2 \cdot f_s = \frac{P_{o, \text{DCM}}}{\eta_{\text{ps}}} \]  

(22)

Since \( I_{\text{peak}}, I_{\text{valley}}, f_s \) and \( \eta_{\text{ps}} \) have been determined at the beginning of the design procedure, \( L_m \) can be calculated.

As mentioned in section E, due to the slope compensation, the peak current at low line is lower than that at high line. So usually the transformer inductance is designed at low line and full load condition. In order to avoid the influence by components parameters variation, 20% margin is usually reserved for maximum output power.

As described in the previous section, the FB voltage reaches its maximum at low line and full load. When the output power is larger than the maximum power that converter can deliver, the FB voltage reaches 3.8V. The internal Over Load Protection (OLP) counter starts. MP110 enters OLP mode and shuts down its switching if the 8192 switching cycles elapse. When the fault disappears, the power supply resumes operation. The OLP delay can be got by the below equation.

\[ T_{\text{Delay}} = \frac{8192}{f_s} \]  

(23)
G. Input Over Voltage Protection Function

MP110 has input over voltage protection function to avoid the input over voltage damage. It can be set as Figure-15.

![Figure-15 Input OVP Circuit](image)

The resistor divider can be set by the equation (24).

$$V_{\text{IN,OVP}} \cdot \frac{R_4}{R_1 + R_2 + R_3 + R_4} = V_{\text{PRO}}$$  \hspace{1cm} (24)

$V_{\text{PRO}}$ (3.1V typical) is protection threshold on PRO. The resistor should be with 1206 package from safety consideration. Generally speaking, each resistor with 1206 package can sustain 200V voltage and 4 resistors are needed if the maximum input voltage is 420Vac or even 440Vac. In order to achieve low no power consumption, total resistance of the resistor divider should be larger than 10MΩ.

In order to filter the noise brought by the resistor divider on PRO, one ceramic capacitor around 1nF is needed to parallel with R4 and it should be placed near the PRO. The input line OVP function can be disabled by shorting the PRO to ground.
H. Transformer Design

H-1. Transformer Core Selection

An appropriate core for certain output power and operating frequency needs to be selected. Ferrite core is usually preferred for Flyback transformer. The core area product (A_E*A_W) which is the core magnetic cross-section area multiplied by window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required A_E*A_W (cm^4) is given by following equation [1]:

\[
A_E \cdot A_W = \left( \frac{L_m \cdot I_{\text{peak}} \cdot I_{\text{rms}} \cdot 10^4}{B_{\text{max}} \cdot K_u \cdot K_j \cdot f_s} \right)^{\frac{1}{2}} \text{ cm}^4
\]

Where \( K_u \) is winding factor which is usually 0.25~0.3 for an off-line transformer. \( K_j \) is the current-density coefficient (typically 400~450 for ferrite core). \( I_{\text{peak}} \) and \( I_{\text{rms}} \) is the maximum peak current and RMS current of the primary inductance, \( B_{\text{max}} \) is the allowed maximum flux density in normal operation which is usually preset to be the saturation flux density of the core material (0.3T~0.35T). \( f_s \) is the switching frequency at low line and full load condition. RMS current is given by following equation.

\[
I_{\text{rms}} = \sqrt{\left( \frac{I_{\text{peak}} - I_{\text{valley}}}{2} \right)^2 + \frac{1}{12} \left( I_{\text{peak}} - I_{\text{valley}} \right)^2} \cdot D
\]

For power supply at DCM, \( I_{\text{valley}} \) equals to 0.

H-2. Primary and Secondary Winding Turns

With a given core size, equation (27) defines a minimum value of \( N_p \) for the transformer primary winding to prevent the core from saturation:

\[
N_p = \frac{L_m \cdot I_{\text{peak}}}{A_E \cdot B_{\text{max}}}
\]

Where:

- \( L_m \) is the primary side inductance of the transformer
- \( B_{\text{max}} \) is the maximum allowable flux density
- \( A_E \) is the effective cross sectional core
- \( I_{\text{peak}} \) is the peak current in the primary side of the transformer

The maximum allowable flux density \( B_{\text{max}} \) should be smaller than the saturation flux density \( B_{\text{sat}} \). Since \( B_{\text{sat}} \) decreases as the temperature increases, which should be considered in the design.

Secondary winding turns \( N_s \) is a function of \( N \) and \( N_p \), which is given by equation (28).

\[
N_s = \frac{N_p}{N}
\]

H-3. Wire Size

Once all the winding turns are determined, the wire size should be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the RMS current value, the length and the width of wire, also the transformer structure.

The wire size could be determined by the RMS current of the winding. For a Flyback converter, the RMS current on primary side is given by equation (26), and the RMS current on secondary side is given by equation (29).
\[ I_{\text{sec rms}} = N \cdot \sqrt{\left(\frac{I_{\text{peak}} + I_{\text{valley}}}{2}\right)^2 + \frac{1}{12} \left(I_{\text{peak}} - I_{\text{valley}}\right)^2} \cdot (1 - D) \] (29)

For Flyback operated at DCM, \( I_{\text{valley}} \) equals to 0.

Then, the wire size required at primary and secondary side is got by equation (30) and equation (31).

\[ S_{\text{pri}} = \frac{I_{\text{pri rms}}}{J} \] (30)

\[ S_{\text{sec}} = \frac{I_{\text{sec rms}}}{J} \] (31)

Here \( J \) is the current density of the wire which is 450A/cm² typically.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire should be less than \( 2 \cdot \Delta d \) (\( \Delta d \): skin effect depth):

\[ \Delta d = \frac{1}{\sqrt{\pi \cdot f \cdot \mu \cdot \sigma}} \cdot 10^3 \text{(mm)} \] (32)

Where \( \mu \) is the magnetic permeability of the conductor, which usually equals to the permeability of vacuum for most conductor, i.e. \( 4\pi \times 10^{-7} \text{ H/m} \), \( \sigma \) is the conductivity of the wire (for copper, \( \sigma \) is typically \( 6 \times 10^7 \text{ S/m} \) at \( 0^\circ \text{C} \), \( \sigma \) will increases as temperature increases, which means the \( \Delta d \) will get smaller).

If the required size of the winding is larger than \( \Delta d \), multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance. The effective cross section area of multi-strands wire or Litz wire should be large enough to meet the current density requirement.

After the wire sizes have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and added together, the area for inter-winding insulation, bobbin and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these inter-winding insulation and spaces between turns. It is recommended that a fill factor no greater than about 30% be used. For transformers with multiple outputs this factor may need to be reduced further.

Based on these considerations, the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, reduction in wire size increases the copper loss of the transformer.

H-4. Air Gap

With the selected core and winding turns, the air gap of the core is given as equation (33):

\[ l_a = \frac{\mu_0 \cdot N_p^2 \cdot A_e}{L_m} - \frac{l_c}{\mu_r} \] (33)
Where $A_e$ is the cross sectional area of the selected core, $\mu_0$ is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m. $L_m$ and $N_P$ is the primary winding inductance and turns respectively, $l_c$ is the core magnetic path length and $\mu_r$ is the relative magnetic permeability of the core material. For Ferrite core, $\mu_r$ is very large, so $l_a$ can be approximately calculated as equation (34).

$$I_a = \frac{\mu_0 \cdot N_P^2 \cdot A_e}{L_m}$$ \hspace{1cm} (34)

I. RCD Snubber Design

There is high voltage spike on the Drain due to leakage inductance of transformer when the MOSFET turns off. If the voltage is higher than voltage rating of MP110, the part may have avalanche damage. Therefore, the voltage spike should be suppressed to an acceptable level. The RCD snubber is usually adopted to suppress the voltage spike. The RCD clamp circuit and key waveforms are shown in Figure-16 and Figure-17 respectively. The RCD snubber circuit absorbs the energy stored in the leakage inductor when $V_{DS}$ exceeds $V_{in} + N^*(V_o + V_F)$. It is assumed that the snubber capacitance is large enough thus its voltage is constant during one switching period.

![Figure-16 Flyback Converter with RCD Snubber](image)
When the MOSFET turns off and $V_{DS}$ is charged to $V_{in}+V_{RO}$, the secondary diode turns on at the same time. The primary current starts to charge $C_{sn}$ through the snubber diode ($D_{sn}$). The voltage stress of MOSFET is clamped to $V_{in}+V_{sn}$. Therefore, the voltage across $L_k$ is $V_{sn}-V_{RO}$. The slope of $i_{sn}$ is given by equation (35).

$$\frac{di_{sn}}{dt} = -\left(\frac{V_{sn} - V_{RO}}{L_k}\right)$$

(35)

Where $i_{sn}$ is the current into the snubber circuit, $V_{sn}$ is the voltage across the snubber capacitor $C_{sn}$, $V_{RO}$ is the reflected output voltage and it is equal to $N^*(V_o+V_F)$. $L_k$ is the leakage inductance of the main transformer. The time $t_s$ is obtained by equation (36).

$$t_s = \frac{L_k}{V_{sn} - V_{RO}} \cdot \frac{i_{peak}}{V_{sn}^2}$$

(36)

$V_{sn}$ should be large enough and it is generally set 1.5~2 times of $V_{RO}$, otherwise the power loss caused by leakage current is too large. Once $V_{sn}$ is determined, the power dissipated in the snubber circuit is obtained by equation (37).

$$P_{sn} = V_{sn} \cdot \frac{i_{peak} \cdot t_s}{2} \cdot f_s = \frac{1}{2} \cdot L_k \cdot \frac{i_{peak}^2}{V_{sn} - V_{RO}} \cdot \frac{V_{sn}}{V_{sn}} \cdot f_s$$

(37)
On the other hand, since the power consumed in the snubber resistor \( R_{\text{sn}} \) is \( V_{\text{sn}}^2/R_{\text{sn}} \), the resistance is obtained by:

\[
R_{\text{sn}} = \frac{V_{\text{sn}}^2}{\frac{1}{2} L_k \cdot I_{\text{peak}}^2 \cdot \frac{V_{\text{sn}}}{V_{\text{sn}} - V_{\text{RO}}} \cdot f_s} \tag{38}
\]

The snubber resistor with the proper rated power should be chosen based on the power loss.

The RCD capacitor influences the voltage ripple of \( V_{\text{sn}} \). Large capacitance leads to small voltage ripple. In general, 5~10% ripple is reasonable. Then the snubber capacitance can be calculated by the equation (39).

\[
C_{\text{sn}} = \frac{V_{\text{sn}}}{\Delta V_{\text{sn}} \cdot R_{\text{sn}} \cdot f_s} \tag{39}
\]

When the input voltage increases, the peak current decreases thus snubber capacitor voltage \( V_{\text{sn}} \) also decreases. The snubber capacitor voltage under high line input can be got by the equation (40).

\[
V_{\text{sn}2} = \frac{V_{\text{RO}} + \sqrt{V_{\text{RO}}^2 + 2 \cdot R_{\text{sn}} \cdot L_k \cdot f_s \cdot I_{\text{peak}2}^2}}{2} \tag{40}
\]

If the converter operates in CCM in high line, the \( I_{\text{peak}2} \) in equation (40) can be got through equation (41).

\[
I_{\text{peak}2} = \frac{P_m \cdot (V_{\text{DC,max}} + V_{\text{RO}})}{V_{\text{DC,max}} \cdot V_{\text{RO}}} + \frac{V_{\text{DC,max}} \cdot V_{\text{RO}}}{2 \cdot L_m \cdot f_s \cdot (V_{\text{DC,max}} + V_{\text{RO}})} \tag{41}
\]

If the converter operates in DCM at high line, the \( I_{\text{peak}2} \) in equation (40) can be got through equation (42).

\[
I_{\text{peak}2} = \frac{2 \cdot P_m}{\sqrt{f_s \cdot L_m}} \tag{42}
\]

Usually the voltage spike caused by leakage inductance is lower than the calculated value due to the influence of RCD diode reverse recovery and parasitic capacitance, thus the snubber design usually needs to be tuned based on the bench test.

Then the peak voltage on Drain is shown as Figure-18 and it can be calculated through equation (43).

\[
V_{\text{ds,max}} = V_{\text{DC,max}} + V_{\text{sn2}} + V_{\text{spike}} \tag{43}
\]

The \( V_{\text{spike}} \) is caused by the stray inductance and generally it is 10V-20V. Make sure the maximum Drain voltage has 10% margin of the breakdown voltage (900V) of MP110.

The Drain-Source Voltage is calculated theoretically. \( R_{\text{SN}} \) and \( C_{\text{SN}} \) should be tuned on bench for better stress performance.
J. Output Diode Design

The maximum voltage supplied on secondary side output diode can be calculated by equation (44).

\[ V_D = \frac{V_{in,\text{max}}}{N} + V_o \]  

(44)

Where \( V_{in,\text{max}} \) is the maximum input voltage, \( N \) is the turn ratio and \( V_o \) is the output voltage.

Generally, the voltage rating of secondary side diode should leave \( \sim 20\% \) margin and the output current should be 50% diode rated current considering thermal performance.

The super-fast diode or Schottky diode is recommended for less power loss and better efficiency.

K. Output Filters Design

The ripple current of the output capacitor can be calculated based on equation (45). The ripple current should be smaller than the rated output capacitor RMS current.

\[ I_{\text{cap,RMS}} = \sqrt{\frac{V_{in,\text{max}}^2 - V_o^2}{I_{D_{\text{RMS}}}}} \]  

(45)

Where \( I_{D_{\text{RMS}}} \) is the RMS current of secondary diode and \( V_o \) is specified as equation (46) and equation (47) for DCM and CCM respectively.

\[ I_{D_{\text{rms}}} = N^2 \cdot I_{\text{peak}} \cdot \frac{1-D}{3} \]  

(46)

\[ I_{D_{\text{rms}}} = N^2 \cdot \left[ \left( \frac{I_{\text{peak}} + I_{\text{valley}}}{2} \right)^2 + \frac{1}{12} \left( I_{\text{peak}} - I_{\text{valley}} \right)^2 \right] \cdot (1-D) \]  

(47)

Where \( D \) is the primary side duty cycle, \( N \) is the turn ratio, \( I_{\text{peak}} \) is the primary side current peak and \( I_{\text{valley}} \) is the primary side valley current at CCM.

The voltage ripple at the output can be estimated by:

\[ \Delta V_o = \frac{L_s \cdot D \cdot T_s}{C_o} + (N \cdot I_{\text{peak}} - I_o) \cdot R_{\text{ESR}} \]  

(48)

Where \( T_s \) is switching period, \( C_o \) is output filter capacitance, and \( R_{\text{ESR}} \) is the effective series resistance of output capacitor \( C_o \). If the electrolytic capacitor is used as the output capacitor, due to its high ESR and...
ESL, a film capacitor or ceramic capacitor is usually adopted in parallel to provide a low impedance current path for high frequency current ripple. In order to further reduce the output voltage ripple, a small LC filter can be inserted between the output capacitor and output terminal. A lower corner frequency means better filter effect but may make system unstable. The corner frequency is usually set at around 1/5-1/10 of the switching frequency.

L. Thermal Performance Check

The total loss of the MP110 is divided into two portions, one is on the internal control circuit and the other is on the power MOSFET. The loss caused by integrated 900V MOSFET is dominant at high line or heavy load condition, so usually the thermal performance can be improved by reducing the MOSFET power loss.

The power loss of the 900V MOSFET is mainly caused by turn-on process at high line and the turn-on loss is proportional to switching frequency. Thus the switching frequency can’t be set too high. The rule of thumb is that if the maximum input voltage is more than 400Vac and output power is equal or more than 5W, the switching frequency should be lower than 100kHz, and ~60kHz is recommended.

In general, 50°C case temperature rise is allowed. If the high switching frequency is necessary or the output power is too high, heat sinks can be adopted to meet the thermal requirement. Four different heat sinks (6 teeth) are listed in Table-1 and the thermal comparison is shown in Table-2. The test condition is: Vin=600Vdc, Vout=12.37V, Iout=0.405A, Pout=5W.

<table>
<thead>
<tr>
<th>Table-1 Heatsink Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>Length</td>
</tr>
<tr>
<td>1# Heatsink</td>
</tr>
<tr>
<td>2# Heatsink</td>
</tr>
<tr>
<td>3# Heatsink</td>
</tr>
<tr>
<td>4# Heatsink</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table-2 Thermal Performance w/i and w/o Heatsink</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Temperature</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>1# Heatsink</td>
</tr>
<tr>
<td>2# Heatsink</td>
</tr>
<tr>
<td>3# Heatsink</td>
</tr>
<tr>
<td>4# Heatsink</td>
</tr>
<tr>
<td>w/o Heatsink</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
M. PCB Layout

The PCB layout has great relationship with the EMI, thermal and so on. Good layout can lead to good EMI performance and thermal performance. In this section one PCB layout is attached. Following guidance should be applied to optimize the PCB layout.

1) Minimize the power loop area. The power loop includes primary side main power loop (Input Capacitor-Transformer Primary Main Winding-Drain-Source-Sensing Resistor-Input Capacitor), RCD snubber loop (Transformer Primary Main Winding-Drain-RCD Diode-RCD Capacitor-Transformer Primary Main Winding), Vcc charge loop (Transformer auxiliary winding-Vcc Diode-Vcc Cap-Transformer auxiliary winding) and the secondary side main power loop (Transformer secondary winding-Output diode-Output cap-Transformer secondary winding). The four loops are marked in the figure with 1, 2, 3 and 4 respectively.

2) The GND of input power loop and control loop should be separated and connected at the negative terminal of input capacitor by one point.

3) The FB and Vcc decoupling capacitor is recommended to place near the chip.

4) Enlarge the Source area for better thermal performance. Drain area shouldn't be too large due to it is jumping point and can influence the EMI performance.

5) The switching point should be placed far away from EMI filter. Or the switching point may couple noise to the input line so that the EMI filter loses some effect.

6) The three outputs should satisfy the insulation requirement.

7) If the heatsink is needed, connect the heatsink with primary side GND.

---

![Figure-19 Triple Outputs Flyback PCB Layout with MP110](image-url)
N. Design Flow Chart

Start

Given the input spec, Vo, Io spec for each output, the estimate efficiency of the circuit get the total output power

Select the input cap
Typically 2-3μF per Watt

Get the minimum and maximum input DC voltage

Determine the reflect output voltage VR0

Estimate the turns ratio of transformer, voltage spike of MOSFET and secondary diode

Determine the switching frequency to get the resistance connects FSET

Determine the input OVP to get the resistance connects PRO

Determine the ratio of ripple and peak primary current Kp at minimum input DC voltage

Get the primary inductance and current sense resistance

Get the primary and secondary peak current and RMS current

Determine the Bmax Get maximum required AP

Select transformer core company and shape

Get the proper transformer core and turns for each winding

Select each coil number and parallel windings

Proper current density?

Y

Estimate the fill factor. Get the required Aw

Enough winding area?

N

Y

According to leakage inductance to get the RCD Snubber

Select the output diode

Select the output filter

Determine if the heatsink is needed

The design is finished

Red Fonts: Input Items
Deep Green Fonts: Results

Figure-20 Flyback Design Flow Chart with MP110
O. Experimental Verification

- A detailed reference design for E-meter power with MP110 is shown in Figure-21.
- The input voltage is 85Vac to 420Vac and three outputs, output1 is 13.5V/0.3A, output 2 is 8V/0.05A and output3 is 8V/0.05A.
The transformer used in this design has a turn ratio of 22:100:13:15:9:9 with 3.4mH primary inductance. The core selected is EE16. The wire structure is shown as Figure-22, Figure-23 and Table-3.

Notes:
- All winding terminals are added tube;
- N5 is flying out from the bobbin, Terminal A is labeled with black and terminal B is labeled with white;
- Remove Pin7 and Pin8;
- Shield the transformer with copper foil and connect it to Pin3;
- Varnish the transformer.

Figure-22 Transformer Connection Diagram

Notes:
- One tape outside of each winding;
- 3mm wall to keep winding at the center of bobbin for better consistency

Figure-23 Transformer Winding Diagram
### Table-3 Transformer Winding Detail Information

<table>
<thead>
<tr>
<th>Winding No.</th>
<th>Tape Layer Number</th>
<th>Start &amp; End</th>
<th>Winding Wire Φ(mm)</th>
<th>Turns</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>1</td>
<td>1→NC</td>
<td>0.18mm * 2</td>
<td>22</td>
</tr>
<tr>
<td>N2</td>
<td>1</td>
<td>2→1</td>
<td>0.15mm * 1</td>
<td>120</td>
</tr>
<tr>
<td>N3</td>
<td>1</td>
<td>4→3</td>
<td>0.15mm * 1</td>
<td>13</td>
</tr>
<tr>
<td>N6</td>
<td>1</td>
<td>5→6</td>
<td>0.30mm * 1 TIW</td>
<td>15</td>
</tr>
<tr>
<td>N4</td>
<td>1</td>
<td>10→9</td>
<td>0.16mm * 1 TIW</td>
<td>9</td>
</tr>
<tr>
<td>N5</td>
<td>1</td>
<td>A→B</td>
<td>0.16mm* 1 TIW</td>
<td>9</td>
</tr>
</tbody>
</table>

To verify design procedure presented in this application note and the performance, a prototype based in Figure-21 is built and tested with specified input/output condition (Input: 85VAC~420VAC; Output1: 13.5V/0.3A, Output2: 8V/0.05A, Output3: 8V/0.05A).
The converter is designed to operate in BCM at 85Vac input and full load while in DCM at high line. Figure-24 and Figure-25 show the current sensing voltage and Drain voltage waveform of primary MOSFET.
Figure-26 shows Burst Mode function of the controller at light load. The MP110 skips switching cycles when the FB voltage decreases lower than the threshold $V_{BURL}-0.5V$. Once the FB voltage increases above the threshold $V_{BURH}-0.7V$, the switching resumes. The FB voltage falls and rises repeatedly. Burst mode operation alternately enables and disables switching cycles of the MOSFET thereby reducing switching loss in the no load or light load conditions.

When output power exceeds the maximum designed output power, feedback loop loses control. Then MP110 enters Over Load Protection (OLP) after counting 8192 switching cycles, Figure-27 shows OLP process.
Figure-28 shows the measured efficiency. From the efficiency curve, the efficiency is still high at light load condition due to decreased switching frequency. Also the power consumption at no load is given in Table-4. Due to the burst mode operation, the power loss at no load condition is below 0.2W, even at high line input.

![Efficiency Chart]

Figure-28 Measured Efficiency of the Flyback Converter

<table>
<thead>
<tr>
<th>Input voltage (Vac, RMS)</th>
<th>90</th>
<th>175</th>
<th>265</th>
<th>355</th>
<th>420</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power loss (mW)</td>
<td>115</td>
<td>117</td>
<td>140</td>
<td>175</td>
<td>198</td>
</tr>
</tbody>
</table>

Table-4 No Load Loss at Different Line Voltage

Also conducted EMI test results of Flyback converter complies with EN55022 with 10dB margin.

![Neutral Wire EMI Chart]

Neutral Wire
230Vac/50Hz

![Line Wire EMI Chart]

Line Wire
230Vac/50Hz

Figure-29 Conducted EMI of the Flyback Converter
The maximum case temperature of MP110 is about 75°C while the ambient temperature is 28°C. The temperature rise is lower than 50°C.

Figure-30 Thermal Performance of the Flyback Converter at Low Line (85Vac), Ta=28°C

Figure-31 Thermal Performance of the Flyback Converter at High Line (420Vac), Ta=28°C
4. BUCK CONVERTER DESIGN PROCEDURE

MP110 can also be configured as Buck converter. Due to Buck converter is much simpler than Flyback converter and if there is no isolation requirement, Buck converter may be a better choice. For the Buck converter configured by MP110, Vcc voltage is supplied by output voltage, so it is recommended that the output voltage must be higher than Vcc lower level at which the regulator switch off (V_{CCL}, 9.0V maximum) and lower than Vcc OVP level (V_{OVP}, 22.5V minimum). If the output voltage is little higher than V_{OVP}, a zener diode is needed.

A. Predetermine the Input and Output Specifications

- Input AC voltage range: Vac(min), Vac(max), for example 85Vac~265Vac RMS
- DC bus voltage range: Vin(max), Vin(min)
- Output: Vout, I_{out}(min), I_{out}(max), P_{out}
- Estimated efficiency: $\eta$. It is used to estimate the power conversion efficiency to calculate the maximum input power. Generally, $\eta$ is set to be 0.7-0.75 for low output voltage applications and 0.75-0.8 for high output voltage applications.

Then the maximum input power can be given as:

$$P_{in} = \frac{P_{out}}{\eta}$$  \hspace{1cm} (49)

The input capacitor selection procedure is similar as we depicted in section 3.A.

B. Determine Switching Frequency and Operation Mode

The thermal of MP110 is mainly caused by the power loss of internal 900V MOSFET. We take two examples for reference and provide the switching frequency design guidance.

The output voltage of application 1 is 12V and the output voltage of application 2 is 24V. The output power of both cases is 5W. The conduction vs. inductance under different switching frequency condition is shown as Figure-32(a).

The conclusion can be drawn from Figure-32(a) that when the output voltage is low (12V), the critical inductance at 220Vac line voltage which makes Buck converter operates in BCM is ~0.46mH. The conduction loss is large when the Buck converter operates in DCM or BCM. So make sure Buck converter works in CCM. While when output voltage is high (24V), the critical inductance is ~1.8mH and conduction loss can be acceptable when Buck converter operates in light DCM.

The switching loss is hard to calculate precisely due to it has great relationship with freewheel diode. Large reverse recovery time means high switching loss, especially when the converter operates in CCM. Ultra fast diode is recommended here. When the converter works in DCM, the switching loss isn’t the dominant. So the switching frequency can be pushed higher for small inductor and tight PCB area.

Figure-32(b) shows the conduction loss comparison with different switching frequency for case 2. Higher switching frequency means the lower conduction loss.
In a word, the CCM is preferred for low voltage/high current application and DCM is preferred for high voltage/low current application. The switching frequency is correspondingly low in CCM considering switching loss.

The Table-5 can be taken as reference for ~5W Buck converter design with MP110.

<table>
<thead>
<tr>
<th>Output Spec</th>
<th>12V/0.42A</th>
<th>16V/0.31A</th>
<th>24V/0.21A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation Mode</td>
<td>CCM@220Vac</td>
<td>Light DCM@220Vac</td>
<td>Light DCM@220Vac</td>
</tr>
<tr>
<td>Switching Frequency (kHz)</td>
<td>25-30</td>
<td>40</td>
<td>70-80</td>
</tr>
<tr>
<td>Inductance (mH)</td>
<td>1-3.3</td>
<td>0.5-0.58</td>
<td>0.5-0.65</td>
</tr>
</tbody>
</table>

C. Inductor and Sensing Resistor Design
Since MP110 operates in PWM mode with internally fixed maximum peak current limit, the maximum output power is determined by the sensing resistor and the inductor. So, it is important to select an appropriate inductor based on the desired output power. The way to calculate the maximum output power capability is described as below.

Different inductance leads to different operation mode. Figure-33 and Figure-34 shows the different operation conditions when the converter delivers maximum power.

![Figure-33 Abnormal Operation Modes](image1)

![Figure-34 Normal Operation Modes](image2)

Figure-33 shows two abnormal operation modes due to improper inductor selection. The inductor of the converter is so small, such as tens of μH, that it makes the current slew rate too fast. As a result, within \( t_{LEB2} \) (Leading edge blanking time of SCP, 600ns typical, in order to avoid the premature termination of the switching pulse due to the parasitic capacitance), the current of MOSFET is larger than the SCP threshold. Thus SCP is triggered and the converter can not work normally, just as Figure-33(a) shows.

With a larger inductance, the internal MOSFET current is lower than the SCP threshold within \( t_{LEB2} \), the SCP is not triggered. But the inductor value is also too small which makes the peak current can be higher than \( I_{pk} \) (Peak current limitation) in the \( t_{LEB1} \) (Leading edge blanking time of peak current limitation, 650ns typical). Then the peak current under this condition can be obtained as:

\[
I_{pk} = \frac{(V_{in} - V_o - V_{on}) \cdot T_{LEB1}}{L}
\]  

(50)
Where $V_{on}$ is the voltage drop on Drain-Source of MP110 when internal 900V MOSFET turns on.

And the maximum power is calculated as:

$$P_{\text{max}} = \frac{1}{2} \cdot L \cdot I_{pk}^2 \cdot f_s \cdot \frac{(V_{in} - V_{on} - V_f) \cdot V_o}{(V_{in} - V_o - V_{on}) \cdot (V_o - V_f)}$$  \hspace{1cm} (51)$$

Where $V_{on}$ is the same as in equation (50) and $V_f$ is the forward drop voltage of freewheel diode.

The inductor is also too small that the peak current is not controlled by peak current limitation under full load. This current waveform is shown in Figure-33(b) and it is not recommended.

Figure-34 shows the three normal working modes. The converter can work properly if the ON time is larger than $t_{LEB1}$.

$$t_{on} = \frac{L \cdot I_{pk}}{V_{in} - V_o - V_{on}}$$ \hspace{1cm} (52)$$

The ON time of freewheel diode can be got by equation (53).

$$t_{off} = \frac{L \cdot I_{pk}}{V_o - V_f}$$ \hspace{1cm} (53)$$

When the sum of ON time and OFF time is less than the switching period, the regulator runs in DCM, while when the sum of ON time and OFF time is equal to the switching period, the regulator runs in BCM. The waveforms are shown in Figure-34 (a) and Figure-34 (b) respectively. With the output current increasing, the operation mode will be CCM, just as shown in Figure-34 (c).

The maximum output can be got when the regulator operates in DCM by equation (57),

$$P_{\text{DCM}} = \frac{I_{pk}}{2} \cdot \frac{T_{on} + T_{off}}{T_s} \cdot V_o$$ \hspace{1cm} (54)$$

$$T_{on} = \frac{I_{pk} \cdot L}{V_{in} - V_o - V_{on}}$$ \hspace{1cm} (55)$$

$$T_{off} = \frac{I_{pk} \cdot L}{V_o - V_f}$$ \hspace{1cm} (56)$$

$$P_{\text{DCM\_max}} = \frac{1}{2} \cdot L \cdot I_{pk}^2 \cdot f_s \cdot \frac{(V_{in} - V_{on} - V_f) \cdot V_o}{(V_{in} - V_o - V_{on}) \cdot (V_o - V_f)}$$ \hspace{1cm} (57)$$

Also, the maximum output power of BCM is the same as regulator operates in DCM.

If the converter works in CCM at heavy load conditions, the ripple current can be got:

$$\Delta I = \frac{V_o - V_f}{L} \cdot T_{off}$$ \hspace{1cm} (58)$$
The average output current under this condition is given as equation (59):
\[ I_{o\_max} = I_{pk} - \frac{1}{2} \cdot \Delta I \] (59)

And the maximum power can be calculated as equation (60):
\[ P_{max} = V_o \cdot I_{o\_max} \] (60)

D. Freewheel Diode

The maximum reverse block voltage of freewheel diode must be higher than the maximum input voltage. For the application of universal input voltage, a diode with 600V reverse block voltage is needed. And the current rating of the diode can be determined by the RMS current.

\[ I_{DCM\_RMS} = I_{pk} \cdot \sqrt{\frac{1}{3} \cdot \frac{I_{pk} \cdot L}{V_o - V_f \cdot T_s}} \quad ----DCM \] (61)
\[ I_{CCM\_RMS} = \sqrt{\left(I_{pk}^2 + \frac{\Delta I^2}{12}\right) \cdot \left(1 - \frac{V_o - V_f}{V_{in} - V_{on} - V_f}\right)} \quad ----CCM \] (62)

Where \( \Delta I \) is the current ripple of inductor, it is equal to \( 2 \cdot (I_{pk} - I_o) \).

The reverse recovery of freewheeling diode affects the efficiency and the circuit operation. So an ultra fast diode is recommended. For DCM, reverse recovery time should be less than 75ns, such as EGC10JH from ZOWIE. For CCM, an ultra fast diode should be used, and the reverse recovery time should be less than 35ns, such as UGC10JH.

E. Output Capacitor Design

The output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated by equation (63) and equation (64):

\[ V_{DCM\_ripple} = \frac{I_o}{f_s \cdot C_o} \cdot \left(\frac{I_{pk} - I_o}{I_{pk}}\right)^2 + I_{pk} \cdot R_{ESR} \quad ----DCM \] (63)
\[ V_{CCM\_ripple} = \frac{\Delta I}{8 \cdot f_s \cdot C_o} + \Delta I \cdot R_{ESR} \quad ----CCM \] (64)

Where \( f_s \) is switching frequency, \( R_{ESR} \) is ESR of output capacitor.

To lower the output voltage ripple, Ceramic, tantalum or low ESR electrolytic capacitors are recommended.

At the output, a dummy load is also required to maintain the output regulation under no-load condition. This can ensure sufficient energy to charge the \( V_{CC} \) capacitor, and to detect the output voltage. Normally a 1mA dummy load is needed and can be adjusted according the regulation. Increasing the dummy load improves load regulation but deteriorates the efficiency and no-load consumption. If the user cares nothing about the output regulation under no-load condition, a Zener diode is recommended for lower no-load consumption.
F. Vcc Power Supply and Power Feedback Circuit Design

The Vcc Power Supply and feedback circuit of Buck converter with MP110 is shown as Figure-35. The Vcc capacitor is directly charged through the red path when freewheel diode conducts. If the output voltage is higher than the rated voltage of Zener diode, Zener diode breaks down and then the FB voltage is regulated by the transistor Q1.

![Figure-35 Vcc Power Supply and Feedback Circuit of Buck Circuit with MP110](image)

F-1. VCC Charge Diode Selection

The diode D1 should have the same voltage rating as the freewheel diode. The current of this diode is very small, so fast and slow diodes such as FR10X and 1N400X can be used. However, in order to obtain a better regulation, charge diode and freewheel diode should have the same forward voltage drop.

F-2. VCC Capacitor Selection

The MP110 consumes milli-amperes current when it is in operation. In order to make sure the Vcc voltage doesn’t drop below Vcc off threshold before the output voltage setup, Equation (65) should be satisfied.

\[
I_{CC} \cdot T_{Start} < C_{Vcc} \cdot (V_{CCH} - V_{CCL})
\]

Where \( I_{CC} \) is the IC consumes current and typically is 1-2mA. \( T_{Start} \) is the startup time. \( V_{CCH} \) and \( V_{CCL} \) is Vcc ON and OFF threshold. Then the Vcc capacitor can be got. Generally, 10μF to 47μF is commended for VCC capacitor. Also a 0.1μF ceramic is commended to parallel with this capacitor.

F-3. Zener Diode Selection

The output voltage reference is implemented by the Zener breakdown voltage. Generally, the voltage rating of Zener diode (Zener 1) should be selected as equation (66).

\[
V_{Zener} = V_O + V_{be}
\]

\( V_O \) is output voltage and \( V_{be} \) is the base-emitter drop voltage of the transistor, the typical value is 0.7V. If the output voltage is little higher than \( V_{CC} \) OVP voltage, a Zener diode (Zener 2) is needed to protect the part enters OVP. The voltage on Vcc must be higher than low level when operation current is maximum and lower than \( V_{CC} \) OVP level when operation current is minimum. The following formula should be satisfied.
\[ V_{\text{Zener}} < V_{\text{OVP}} \]  
\[ V_o > V_{\text{CCL}} + I_{\text{CC_max}} \cdot R1 \]

### G. Thermal Performance Check

MP110 has an internal OTP function. When the junction temperature of IC increases to 150°C, it triggers over temperature protection. Please avoid MP110 enters OTP during normal operation.

For example, the maximum allowed junction temperature is \( T_b \) (Normally 125°C). And the maximum ambient temperature for normal application is \( T_a \). So the maximum junction temperature rise should not be bigger than \( \Delta T = T_b - T_a \). The junction-to-ambient thermal resistance \( \theta_{JA} \) is 68°C/W. The maximum power loss of IC is:

\[
P_{\text{max_loss}} = \frac{T_b - T_a}{\theta_{JA}}
\]

The power loss of MP110 mainly caused by internal 900V MOSFET. The conduction loss of MOSFET is easy to calculate and the result is close to the real value.

![Figure-36 DCM and CCM Operation Current of MP110](image)

The MOSFET current under DCM and CCM is shown as Figure-36. The duty cycle when Buck converter operates in DCM and CCM can be calculated as:

\[
D_{\text{DCM}} = \frac{I_{pk} \cdot L}{(V_{in} - V_{on}) \cdot T_s}
\]

\[
D_{\text{CCM}} = \frac{V_o - V_f}{V_{in} - V_{on} - V_f}
\]

The RMS value of current in MOSFET can be obtained as:

\[
I_{\text{RMS, DCM}} = I_{pk} \cdot \sqrt{\frac{D_{\text{DCM}}}{3}}
\]
The conduction loss of MOSFET is:

$$P_{\text{MOS,con}} = I_{\text{RMS}}^2 \cdot R_{\text{ON}}$$  \hspace{1cm} (74)$$

Please note that the $R_{\text{ON}}$ is the ON resistor of MOSFET at its operation junction temperature.

As depicted in section 4.B, the switching loss of Buck converter has great relationship with reverse recovery of freewheel diode. So the switching loss is hard to calculate accurately. It is better to estimate the loss by capturing relative voltage and current waveforms.

![Figure-37 Switching Loss of Buck Converter at High Line](image)

Normally conduction loss is dominant at low line and switching loss is dominant at high line. Please check the loss pointedly. There should be a tradeoff between loss and switching frequency.

The power loss of internal controller can be calculated as:

$$P_{\text{IC}} = V_{\text{CC}} \cdot I_{\text{CC}}$$  \hspace{1cm} (75)$$

Where $I_{\text{CC}}$ is the operation current under full load condition.
H. Design Flow Chart

Start

Given the input spec, 
Vo, Io spec for each output, the estimate efficiency of the circuit get the total output power

Select the input cap 
Typically 2-3uF per Watt

Get the minimum and maximum input DC voltage

Determine the operation mode to get the inductor and sensing resistor

Get the freewheel diode

Get the output capacitor

Select the feedback circuit parameters

Determine if the heatsink is needed

The design is finished

Figure-38 Buck Converter Design Flow Chart with MP110

I. Experimental Verification
A Buck converter using MP110 as a design example has been built and tested (Input: 85VAC~265VAC; Output: 12.5V/0.4A). The key components value in the circuit is calculated based on the above section and the circuit is shown in Figure-39.

Figure-39 Buck Converter with MP110
The converter is designed to operate in CCM both at low line and high line. At light load, MP110 enters switch skipping mode for better efficiency and when the load increases, MP110 operates in PWM. Figure-40 and Figure-41 show the Drain-Source current and voltage waveforms.

Figure-40 Operation Waveforms when the Buck Converter Operates at Low Line (85Vac)

Figure-41 Operation Waveforms When the Buck Converter Operates at High Line (265Vac)
Figure-42 shows the measured efficiency. From the efficiency curve, the efficiency is still high at light load condition due to decreased switching frequency. Also the power consumption at no load is given in Table-6. Due to the burst mode operation, the power loss at no load condition is very small, even at high line input.

![Efficiency vs. Load Current](image)

Table-6 No Load Loss at Different Line Voltage

<table>
<thead>
<tr>
<th>Input voltage (Vac, RMS)</th>
<th>90</th>
<th>115</th>
<th>230</th>
<th>265</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power loss (mW)</td>
<td>48.3</td>
<td>50.8</td>
<td>59.7</td>
<td>61.1</td>
</tr>
</tbody>
</table>

It can be predicted that the output voltage at no load or light load condition is higher than it at heavy load condition. The output voltage has about 0.8V variation compared between no load and full load condition.

![Line Regulation](image)

The Buck converter is not recommended to be used in high output power applications, because its
primary side RMS current is larger than that of a Flyback converter, and also it has larger turn-on loss due to reverse recovery of freewheel diode. Figure-44 shows the thermal performance of MP110 used in 5W Buck design with 30kHz switching frequency. The case temperature rise is nearly 65°C.

![Thermal Performance of Buck Converter, Ta=30°C](image)

(a) Vin=85Vac  
(b) Vin=265Vac

Figure-44 Thermal Performance of Buck Converter, Ta=30°C
5. REFERENCES