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APPLICATION NOTE

**Low Cost 1000 Watt 300 Volt
RF Power Amplifier for 27.12MHz**

Low Cost 1000 Watt 300 Volt RF Power Amplifier for 27.12MHz

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ABSTRACT

This paper describes the design, development, and performance of a low cost, high-efficiency, 1000 Watt RF power amplifier (PA) for 27.12 MHz, operated from a 300VDC supply. The PA is built around a "symmetric Pair" of low cost RF power MOSFETs from Advanced Power Technology (APT). These transistors are from a new generation of high quality, commercial, HF/VHF high voltage silicon devices, in TO-247 packages. The paper addresses both the theoretical design and physical construction of the amplifier, along with a technical description of the RF power transistors themselves.

INTRODUCTION

Transistorized RF Power Amplifiers operate from a low voltage DC source, usually about 50V or less. It is common to use a DC to DC converter rather than a linear regular to increase the system efficiency. This supply requires a down regulator when operated from AC mains and it is a significant portion of the overall cost of the RF amplifier system.

As a result of IEC1003-2 and its predecessor IEC555, all electronic equipment sold in Europe with a power drawing more than 250W from the mains will require power factor correction (PFC). The addition of a PFC preregulator to the power amplifier system could add 50 to 100% to the cost of the power supply portion. This requirement for power factor correction is soon to follow in the USA and the rest of the world.
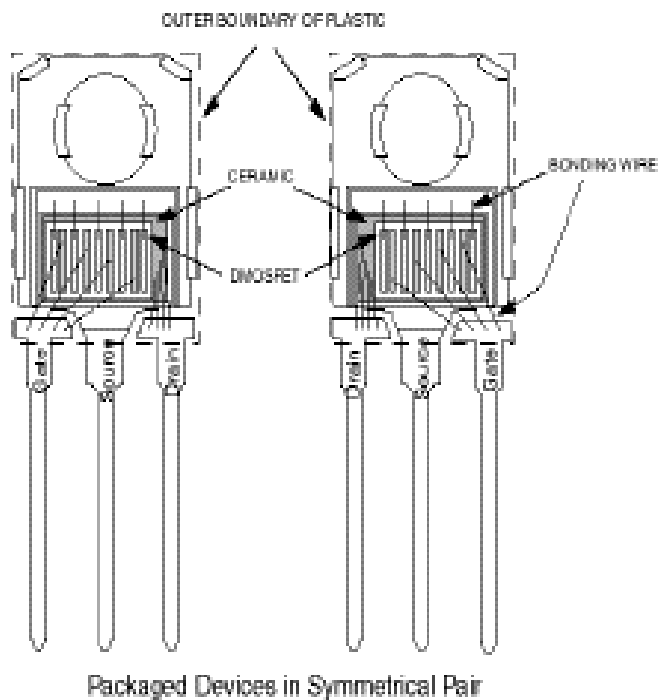
The new high voltage RF MOSFETs from Advanced Power Technology (APT) make possible an RF amplifier design which can be operated at 300V, which then permits the amplifier to be connected directly to a single stage PFC regulated power supply and eliminates the additional DC to DC converter, reducing the cost of the RF amplifier system. The new devices, like their predecessors, utilize the high performance of APT's Power MOS IV® technology, and the "symmetric pair" TO-247 plastic package.

DEVICE DESIGN AND FABRICATION

The device used in this amplifier is a vertical DMOS transistor 340 mil X 200 mil in dimension. The chip layout employs multiple gate and source bonding strips which reduce parasitic lead inductance of the connections to the package terminals. The housing, chosen for purposes of economy, is the standard TO-247 plastic package in the common source configuration, i.e., the backside of the leadframe is connected to the source of the DMOS transistor. This is accomplished by inserting an insulating ceramic substrate between the chip and the leadframe to isolate the drain which is on the backside of the silicon chip from the leadframe and then connecting the source to the leadframe through wire bonding. The insulating substrate is BeO measuring 425 mil X 250 mil in dimension and 25 mil in thickness with metallization. This is the largest size that can be enclosed and sealed by the plastic molding compound at the periphery of the package. The source and gate metal strips are 20 mil wide and 10 um thick and are along the width of the chip so minimal propagation delay and uniform conduction at RF can be achieved within the chip. This is done for thermal, electrical and reliability considerations and provides a uniform power dissipation across the entire device active channel area.

Figure 1.
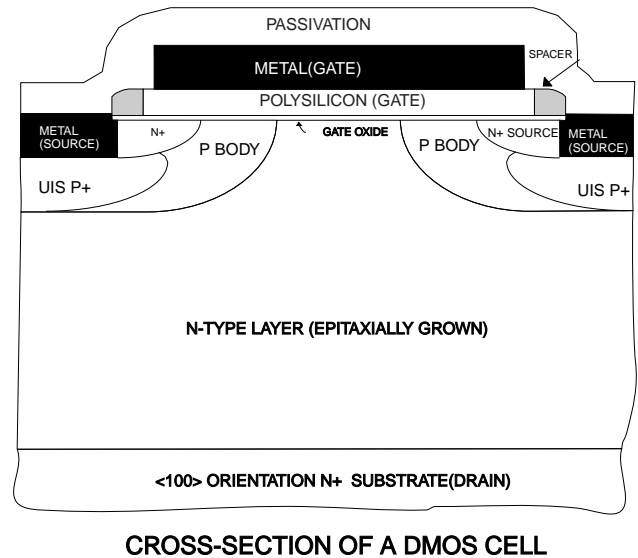

Packaged Devices in Symmetrical Pair

As shown in Figure 1, due to the gate bonding post location of the standard TO-247 package leadframe, the gate bonding wires are longer than the source wires. This adds inductance to the input circuit and increase the difficulty of matching to the driver circuit. Given this standard leadframe, it is necessary to make the gate bonding wires equal in length as shown so equal gate drive to all portions of the chip is maintained. This concept of maintaining uniform gate drive and power dissipation is further enforced through using thick 10 um Al metal on the silicon device for the gate and source bonding strips.

Fabrication of the DMOS transistor follows APT's patented open-cell self-aligned technology with interdigitated gate and source fingers running perpendicular to the bonding strips and parallel to the long dimension of the chip. The resulting device is represented in Figure 2 in cross-section along a line parallel to the gate and source bonding strips. The channel gate oxide for the devices tested is ~1600Å and the body diffusion for the DMOS is ~4 ums. Gate delay is minimized using this technology

due to the extremely low internal gate resistance from the metal atop the polysilicon gate.

Figure 2

CROSS-SECTION OF A DMOS CELL

AMPLIFIER DESCRIPTION

The amplifier is a 1000 Watt, 27.12MHz design operating in class C with a 300VDC power supply. The DC to RF efficiency of the amplifier is greater than 70 percent. The power amplifier is built around two "symmetric pair" of ARF446/ARF447 900V RF power MOSFETs in TO-247 plastic packages. Internally, the devices are electrically identical. They are packaged in "mirror image" pairs to facilitate a symmetrical layout that helps maintain the electrical symmetry and low source-to-source impedance required for push-pull or parallel operation. Figure 3 shows the circuit diagram of the 27.12 MHz amplifier, with the parts list given in Table 1.

The amplifier has the classical push-pull configuration of a straight forward nature. It uses a simple L-C network for input impedance matching with transformer coupling to achieve the required complementary gate drive signals. Because of the fairly high output capacitance of the devices, a wideband output transformer output circuit is not used. A series inductor cancels the effective series equivalent output capacitance and transforms the effective series impedance of each

drain to approximately 10 ohms. The bifilar-wound RF choke serves the dual purpose of impedance transformer and DC power supply decoupling. A conventional coaxial balun transforms the balanced push-pull signal to a single ended. Since the source impedance is not exactly 50 ohms and the balun provides some transformation, the tuned network at the output is needed to secure an optimum match to a 50 ohm load.

Because they can be mounted symmetrically in a common source configuration, it is easy to make short, low inductance interconnections using the ARF446/ARF447 devices. The frequency response of the output circuit is improved with minimum stray inductance due to the short source interconnections[2].

The amplifier is operated directly from the 300VDC power supply, eliminating the DC-DC converter, and is constructed on a heat sink sized for proper dissipation at the expected power levels. Figure 4 shows the component placement on the PC board and heat sink. The common source design of the package allows the device mounting to be accomplished without an insulator thus allowing good heat transfer to the heat sink with the use of thermal grease.
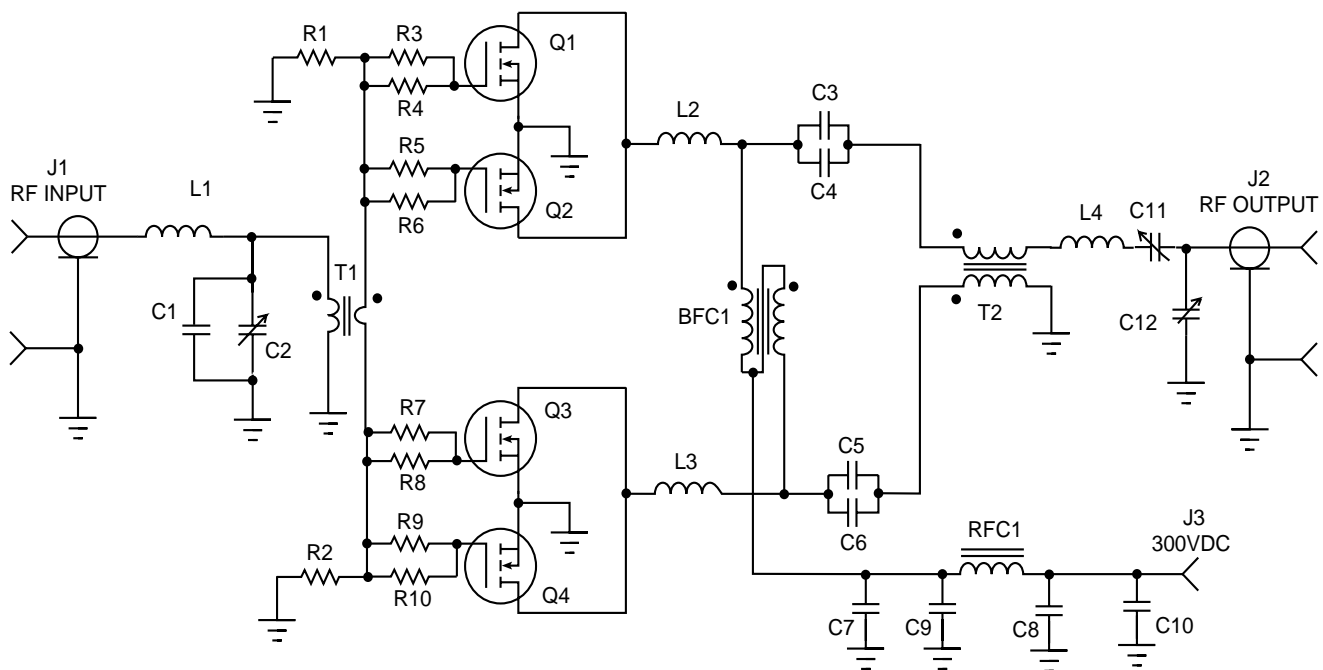

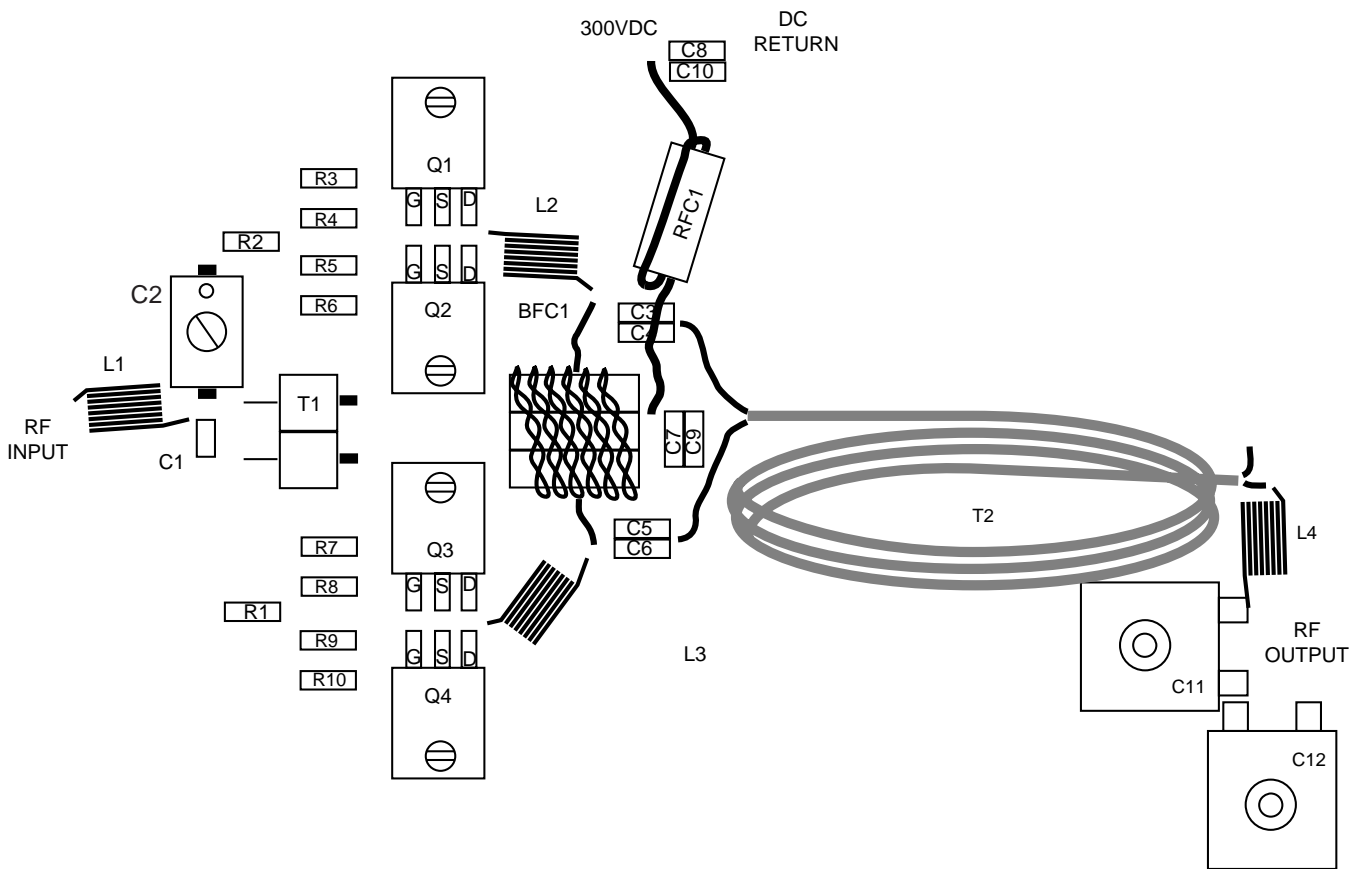**Figure 3. Circuit Diagram of the 1000 Watt Class C Amplifier**

Figure 4. 1000 Watt Class C Power Amplifier Layout

Part Number	Description
R1, R2	1000ý 1W
R3-R10	1ý 2W surface mount 5%
C1	100pF Silver Mica Capacitor
C2	40-200 pF Mica Compression Trimmer Capacitor, Arco 425
C3-C8, C13, C14	0.01µF Disk Ceramic
C9, C10	0.001 Disk Ceramic
C11	250-480pF Mica Compression Trimmer Capacitor, Sprague GME 90901
C12	95-230pF Mica Compression Trimmer Capacitor, Sprague GME 90501
Q1, Q3	ARF446
Q2, Q4	ARF447
L1	.470µH 5.5t, #18AWG enam .438" dia
L2, L3, L4	0.145µH: 3.5T, #14AWG, ID=0.438
RFC1	2T, #18 PTFE on a Fair-Rite #2643665702 shield bead, μ_i=850
T1	4:1 conventional transformer; pri: 2T #18 stranded PTFE coated wire, sec: 1T #14 tinned braid on two Fair-Rite #2643540002, µi=850
T2	1:1 (Z) coaxial balun transformer; 24 inches RG303 PTFE Coax formed into a 3 T, 2.5" dia.
BFC1	6T, #24 twisted pair enamel wire on three stacked Fair-Rite 596118021 toroids.

Table 1. Parts List for the 1000 Watt Power Amplifier

INPUT NETWORK

The input network transforms the MOSFET gate impedance up to the 50ý impedance to the driver source and provides the balanced drive required for push-pull operation. Most of the impedance transformation to the gates is provided by the 4:1 ferrite bead transformer. The input L-network comprised of capacitors C1 and C2 and inductor L1 provide the means for a perfect match at the operating frequency.

Transformer T1 provides a 4:1 impedance transformation of the MOSFET input impedance. It is constructed using two Fair-Rite cores #2643540002, μ=850 with 2 turns of #18 stranded PTFE coated wire on the primary and 1 turn of .25" copper braid on the secondary. The secondary feeds the gates of the MOSFETs through resistors R3 through R10. Resistors R1 and R2 provide the MOSFETs with a DC ground reference to insure the gates do not float to a DC potential thus unbalancing the amplifier bias points. The parallel resistors, R3-R4, R5-R6, R7-R8 and R9-R10, in series with the gates of the MOSFET de-Q the input. They are used to prevent a possible VHF emitter-coupled multivibrator oscillation which can occur when paralleling MOSFETs. They also reduce the available gain by about 5dB which promotes stability. At this frequency and impedance level, ferrite beads are not appropriate for this purpose!

The input impedance of each FET is 0.1 -j 3.9 at 27 MHz, approximately 1500pF in series with less than 0.1 ý. Even with an additional 0.5ý in series, this is very low and any circuit trace adds significant inductance. Acutally, a little series inductance will help the match but it must be symmetrical. When laying out the circuit board extreme care must be taken to assure each of the four FETs has exactly the same gate trace length back to the secondary of the input transformer. Otherwise, significant imbalance due to poor drive sharing will result. This has a direct effect on the efficiency of the amplifier.

It is also important to attend to the grounding of the input components. With the gate current approaching 4 A, ground loop currents make proper ground layout critical. A double sided printed circuit board with the bottom essentially intact is recommended.

The input impedance is not constant over the range of output power. From zero drive through the level where output power appears up to full output, the input impedance moves through a fairly large range. This is a function of the Miller capacitance, Crss. Depending on the characteristics of the driver, the output power can appear to 'snap on' suddenly as the drive is increased if the input network has been previously adjusted for a good match at full output. This can be a little disconcerting, but it is the normal result of interaction between the driver and the load. The use of the matching transformer improves this effect but does not completely eliminate it.

OUTPUT CIRCUIT

The 300VDC power input is delivered through a balanced feed choke BFC1. The choke is designed to create a zero DC magnetic bias in the core when both transistors draw the same average current. With the devices operating 180 degrees out of phase, the windings present a high impedance at 27.12MHz to the drain of each MOSFET. It also acts as a 4:1 impedance trasnformer which greatly simplifies matching the drain impedance to 50ý. The choke is constructed by winding 6 turns of #24 twisted pair (approximately 5 twists per inch) solid enamel wire around three stacked Fair-Rite toroids # 5961001801, μ_i=125.

The output of the power devices is coupled to the output balun through two 145 nH inductors. The balun is a coaxial 1:1 conventional transformer. A three wire balun was evaluated but at this frequency the three turn coil of coax has more than enough common mode impedance to work alone as a balun. The balun is constructed from 24" of RG-303 50ý PTFE coax cable by forming it into a coil of 3 turns approximately 2.5 inches diameter. For best efficiency, a low Q matching network consisting of C11, C12 and L4 provides an exact match to 50

Ohms. Because the output impedance at the input of the balun is not exactly 50 ohms, some SWR exists on the coax. The calculated loss in the coax is .03 dB or less than 1%.

No additional output filtering was needed in the test amplifier, which has the third harmonic 58db down and the second harmonic 45db below the 1000 watt output power level.

PERFORMANCE MEASUREMENTS

The amplifier was operated under two conditions. First the amplifier was driven with a 27.12MHz RF signal, modulated by a 1kHz square wave, at a 50% duty cycle, up to a peak power out of 1600W. Then the amplifier was driven with a 27.12MHz CW RF signal up to a continuous power out of 1200W. Due to the close correlation of the modulated data and the CW data it was concluded that there is significant thermal margin from using four devices at 1000W CW.

Figures 5 through 8 show the performance data for this amplifier. Figure 5 is a plot of P_{in} versus P_{out} and Figure 6 shows gain versus P_{out}. The curves show the classical class C characteristics, with low gain at low power output, improving as the output power increases. The gain peaks over 19 dB when the amplifier output is between 400W and 600W, with a roll-off to 17.5dB at 1600W. In a class C amplifier there is a tradeoff between maximum output power and efficiency. Less drive will produce higher gain but at a reduced efficiency, approximately 60% for 20 dB gain. A maximum efficiency of 75% percent was obtained at 1250W output. Slightly different tuning of the output matching network can adjust the load line to produce optimum efficiency at 1KW. For the purposes of this design article, the goal was maximum power performance. In a practical commercial application however, some of the output power rating should be traded for an increased ruggedness margin.
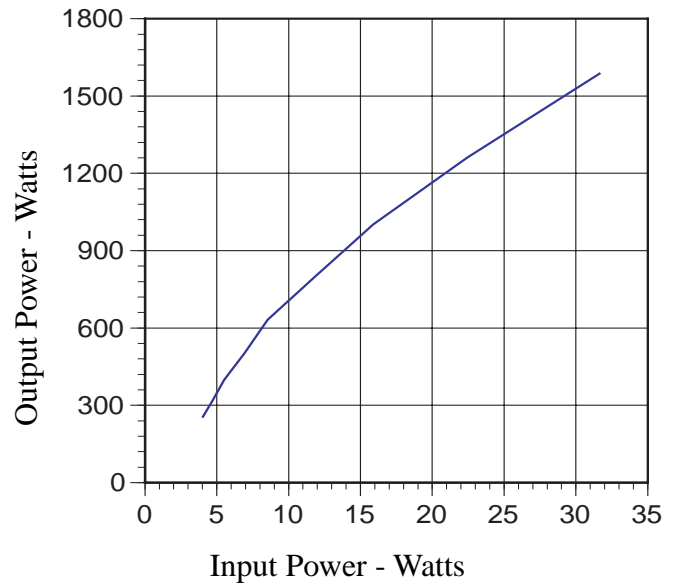

Figure 5. Input Power Versus Output Power

Efficiency versus P_{out} is shown in Figure 7. As would be expected in class C, the efficiency is over 50% at power output above 300W. The efficiency rises to 70.2% at 800W, continuing to 74% at 1000W output. Figure 8 shows total amplifier power dissipation versus P_{out}. The heat sink and fan used for the prototype amplifier were barely adequate for a KW CW operation. Heating of the devices causes a rise in $R_{ds(on)}$ which can be observed as a slight reduction in gain and efficiency with time. With suitable changes in the drain load impedance, 50% pulsed operation up to 2200W peak, and 20% pulsed duty cycle operation up to 5KW peak was obtained with similar efficiencies.
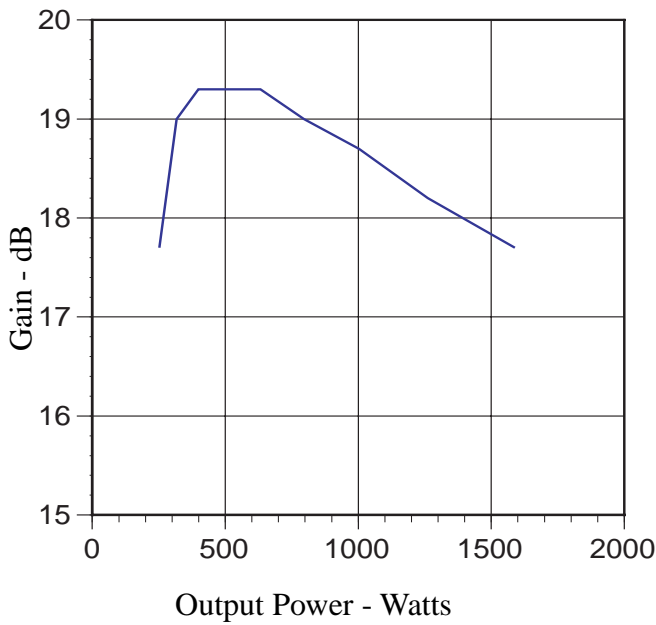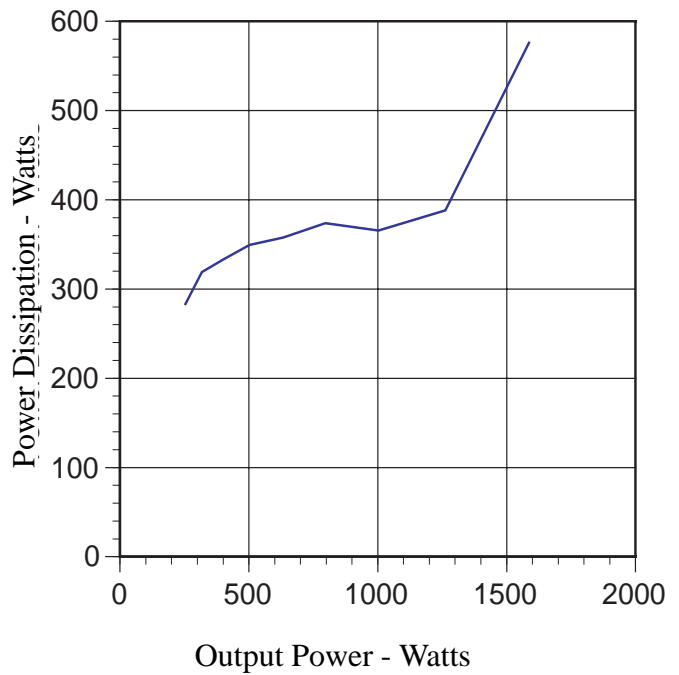
Figure 6. Gain Versus Output Power

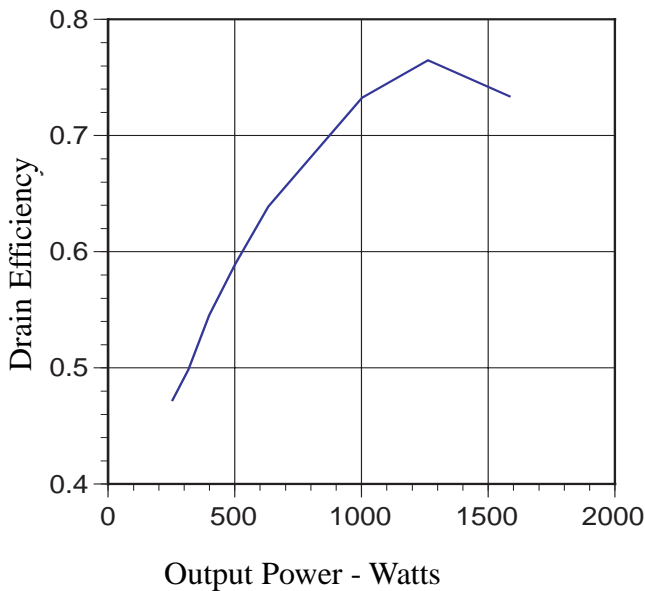**Figure 8. Total Amplifier Power Dissipation Versus Output Power**

Figure 7. Efficiency Versus Output Power

CONCLUSIONS

This paper focuses on recent breakthroughs in commercial solid state RF power device and circuit technology. The high performance low cost components and circuits described, make it possible to engineer solid state (1,000 watt or more) 27.12 MHz power supplies costing much less than an equivalent tube RF power supply or one based on conventional low voltage ceramic/gold packaged RF transistors.

The combination of high voltage operation with high gain, and efficiencies of well over 70 percent, makes this technology exciting just for performance alone. Blending that performance with component costs that allow for multi-kilowatt 27.12MHz amplifiers to be built at less than $0.25 per watt, results in the first real breakthrough in commercial HF power device technology in over a decade. This is only a beginning, in that the commercial technology detailed in this paper will quickly evolve into solid state devices and circuits for even higher frequency, power, and operating voltages.

APT9701

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[2] H. O. Granberg, "Good RF Construction Practices and Techniques," Motorola Application Note AR164, Motorola RF Device Data, Volume II, DL110, Rev. 4.

[3] Ken Dierberger, Denis Grafham, "Design of a 3000 Watt Single MOSFET Power Factor Correction Circuit", APT Application Note APT9303.

[4] H. O. Granberg, "Broad Band Transformers and Power Combining Techniques for RF," Motorola Application Note AN749, Motorola RF Device Data, Volume II, DL110, Rev. 4.

[5] Rudy Severns, et al, "Parallel Operation of Power MOSFETs" "Anomalous Oscillation and Turn-Off Behavior in a Vertical Power MOSFET," MOSPOWER Applications Handbook, Siliconix Inc., 1984.

[6] William E. Sabin, Edgar O. Schoenike, et al, "Single Sideband Systems and Circuits," McGraw-Hill 1987.

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